Quest Journals
Journal of Electronics and Communication Engineering Research
Volume 2 ~ Issue 3 (2014) pp: 07-16
ISSN(Online) : 2321-5941
www.questjournals.org

Research Paper

Low Power and High Performance Full Adder in Deep Submicron Technology

Bamin Gambo, Lod Tapin, Saratchandra Hanjabam
NERIST, Arunachal Pradesh, India

Received 21 February, 2014; **A**ccepted 15 March, 2014 © The author(s) 2014. Published with open access at **www.questjournals.org**

ABSTRACT:- The leakage power dissipation problem of electronics systems has attracted a lot of attention from engineers and researchers over the years. Increasing leakage current in deep-sub micrometer regimes is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power, especially for low-power applications. This work presents the performance of different full adders in deep-submicron using 45nnm, 65nm and 90nm technology. Finally, the paper explores different circuit techniques to estimate the leakage power consumption has been presented. An illustrative example has been provided to demonstrate the design and simulation of CMOS with various technologies using DSCH and MICROWIND program.

Keywords: *full adder, deep-submicron DSCH, MICROWIND, dynamic power dissipation, static Power dissipation, propagation delay.*

I. INTRODUCTION

Rapid growth in semiconductor technology has led to shrinking of feature sizes of transistors using deep submicron (DSM) process. Modern portable battery operated devices such as cell phones, laptops; PDAs are particularly affected by this as high power dissipation reduces battery service life. Thus, power dissipation has now become a vital design metric. Until recently, dynamic or switching power component dominated the total power dissipated by an IC. However, in DSM regime static or leakage power becomes a considerable proportion of the total power dissipation. Hence, this necessitates the need for robust techniques to reduce this leakage power dissipation. To this effect, several techniques have been proposed that efficiently minimize leakage power dissipation.

Many researchers have been done in the past about low power and high performance Full adders. [1] Reviews various transistor intrinsic leakage mechanisms, including weak inversion, drain-induced barrier lowering, gate-induced drain leakage, and gate oxide tunneling. Channel engineering techniques including retrograde well and halo doping are explained as means to manage short-channel effects for continuous scaling of CMOS devices. Finally, they explored different circuit techniques to reduce the leakage power consumption.
[2] They further describe simulation experiments that compare the surveyed full-adder cells. The experiments simulate all combinations of input transitions and consequently determine the delay and power consumption for the various full-adder cells. Moreover, the simulation results highlight the weaknesses and the strengths of the various full-adder cell designs. In their study they used ten of the recently published full-adder cells, from conventional CMOS to inventive XOR-based adders. They believe that for the comparison of power and delay to be fair, they did not size any transistor and overlook some of the failures.
[3] After analyzing various leakage reduction techniques, concluded that there is a strong correlation between the three performance metrics: leakage power, dynamic power and propagation delay. Optimizing for one metric leads to a compromise of the other metrics. It can be concluded that super cutoff CMOS scheme provides efficient leakage power savings in standby mode and forced stacking is a very effective leakage power saving scheme for active mode of operation. However, if propagation delay is the main criteria, it is recommended that a single sleep transistor based circuits are used in standby mode, though leakage savings of up to an order of magnitude is sacrificed. In active mode of operation, the sleepy stack based approach is suitable for faster circuit operation. Based on this work, a designer or an automation tool would be able to select the appropriate leakage control technique for a particular application.

*Corresponding Author: Bamin Gambo
NERIST, Arunachal Pradesh, India

[4] Presented a two new low-power, and high-performance 1- bit Full Adder cells in there paper. These cells are based on low-power XOR/XNOR circuit and Majority-not gate [1]. Majority-not gate, which produces Cout (Output Carry), is implemented with an efficient method, using input capacitors and a static CMOS inverter. This kind of implementation benefits from low power consumption, a high degree of regularity and simplicity. They compared with eight state-of-the-arts 1-bit Full Adders and two proposed Full Adders. This was than simulated with HSPICE using 0.18µm CMOS technology at several supply voltages ranging from 2.4v down to 0.8v. Although low power consumption is targeted in implementation of their designs, simulation results demonstrate great improvement in terms of power consumption and also PDP.
[5] The 8T Full Adder technique has been used for the generation of XOR function. They compared twelve state-of-the art 1-bit full adders and one proposed full adder are simulated with HSPICE using 0.18µm CMOS Technology at 1.8V supply voltage. They compared the dynamic power, static power, power delay product and are occupied by the cell of all state of art of designed full adder and the design adder.

They suggested that optimizing the transistor size in each stage the power and delay are minimized. Simulation results show great improvement in terms of Power-Delay-Product (PDP). They compared the various structures, of typical Full Adder in 8T logic, which embodies only 8 transistors and the number of interconnections between them is highly reduced. Having each transistor a lower interconnection capacitance, the W/L can be close to the minimum value and the power consumption is decreased. The Eight state of the art 1 bit full adder cells including FA24T, Bridge, CPL, DPL, Hybrid, N-Cell1, mod2f and N-10T were simulated with HSPICE with their prototype design to address the dynamic power, static power and power delay product for the adders.
[6] In order to achieve lower static power consumption, one has to sacrifice design area and circuit performance. In their paper, they propose a new method to reduce static power in the CMOS VLSI circuit using Variable Body Biasing technique without being penalized in area requirement and circuit performance. They measured static power consumption, dynamic power consumption, propagation delay and area for five design approaches, which are sleep, sleepy stack, dual sleep, dual stack and variable body biasing approach. They concluded that it gives the CMOS circuit designers another option in designing integrated circuits more efficiently.
[7] Paper focuses on method to reduce leakage power consumption of an 8kbit SRAM by employing techniques like power gating. The main technique used in power gating is the use of sleep transistor. [8] CMOS circuit design; layout and simulation are discussed here.
In this paper, dynamic power dissipation, static power dissipation and propagation delay are estimated for Conventional full adder, Bridge adder, CPL adder, FA24T adder, hybrid adder, N-10T adder, mod2f adder and N-cell adder using 45nm, 65nm and 90nm technologies.
The paper is organized as follows. Section I presents introduction to deep-submicron. Section II presents eight states of full adder cells. Section III presents the testing of proposed design techniques. Section IV shows the comparison of different design techniques with respect to different parameters. Section V Conclusion and references of proposed design techniques.

II. DSCH and MICROWIND SCHEMATIC OF EIGHT STATE FULL ADDER CELLS

[4] Evaluated dynamic power dissipation, static Power dissipation and propagation delay using HSPICE software using 0.18µm technology. But In this paper the dynamic power dissipation, static Power dissipation and propagation delay of different static CMOS logic cells are evaluated using DSCH and MICROWIND software using 45nm, 64nm and 90nm technology which are used to implement low-power and high performance 1-bit full adder cell of all the eight state-of-art full adder cells.

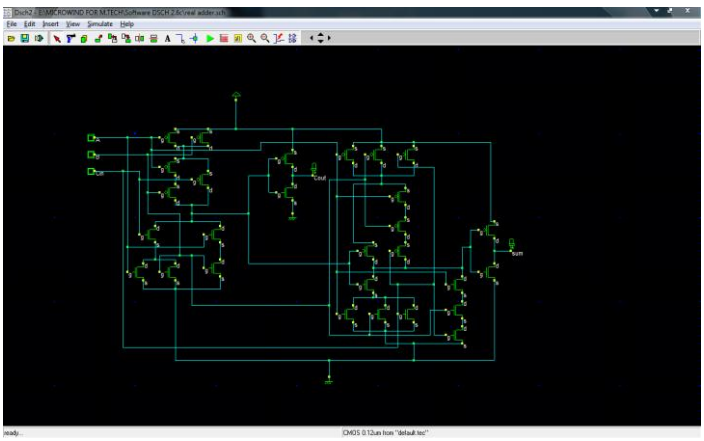


Fig 1.1: Conventional CMOS full adder

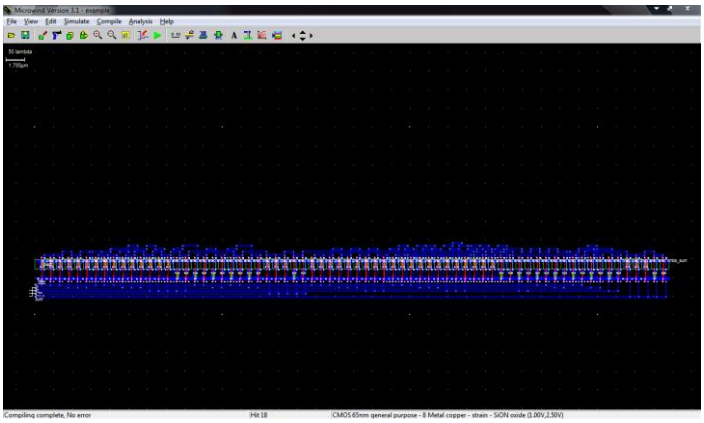


Fig 1.2 MICROWIND result of 1 bit full adder

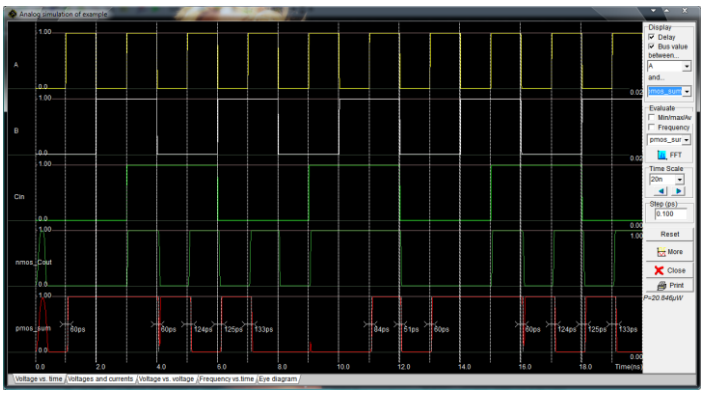


Fig. 1.3 Output graph of CMOS full adder

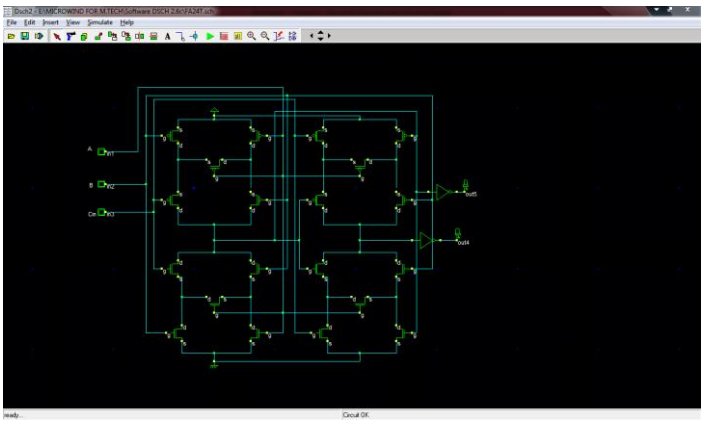


Fig.1.4 DSCH Schematic of FA24T full adder

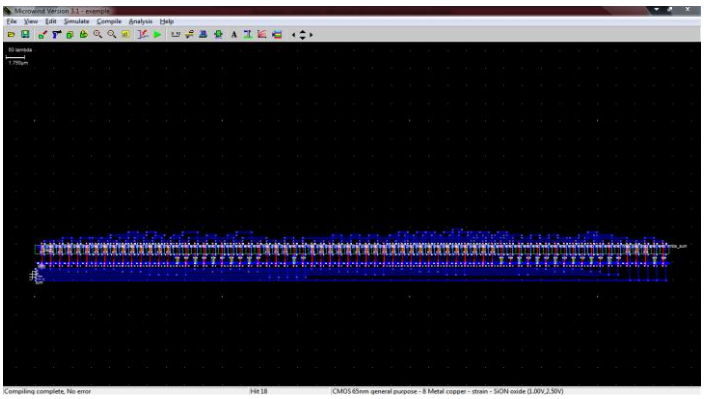


Fig.1.5 MICROWIND Schematic of FA24T full adder

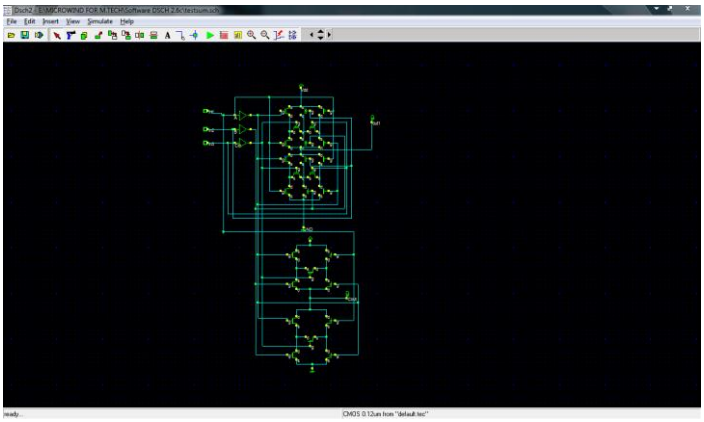


Fig.1.6 DSCH Schematic of Bridge full adder

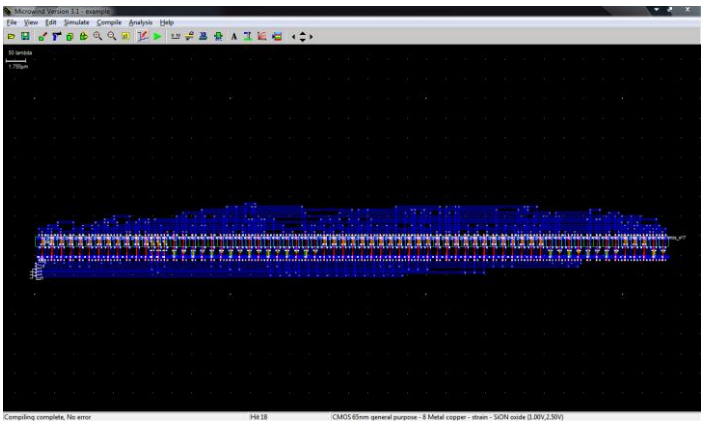


Fig.1.7 MICROWIND Schematic of Bridge full adder

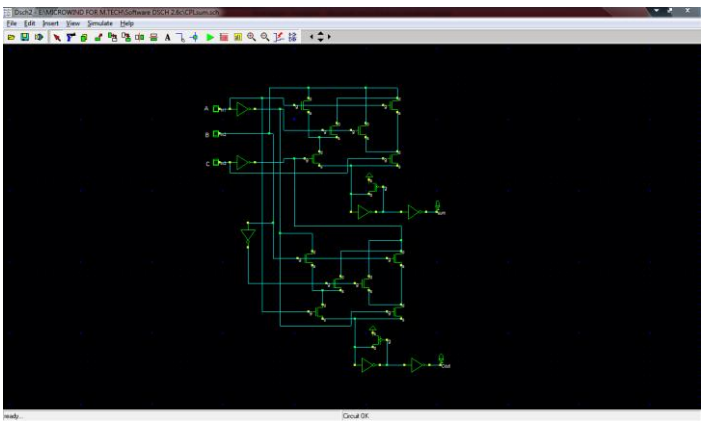


Fig.1.8 DSCH Schematic of CPL full adder

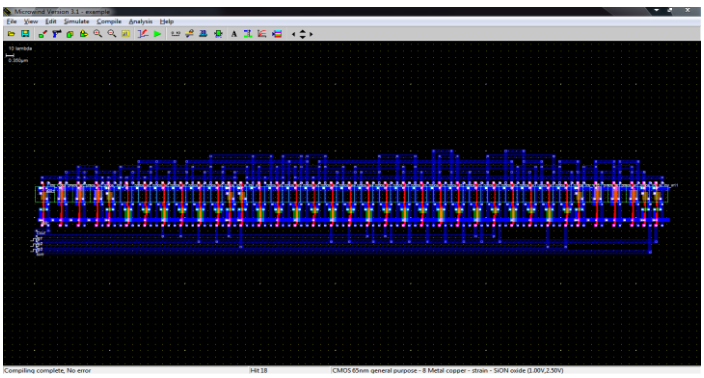


Fig.1.9 MICROWIND Schematic of CPL full adder

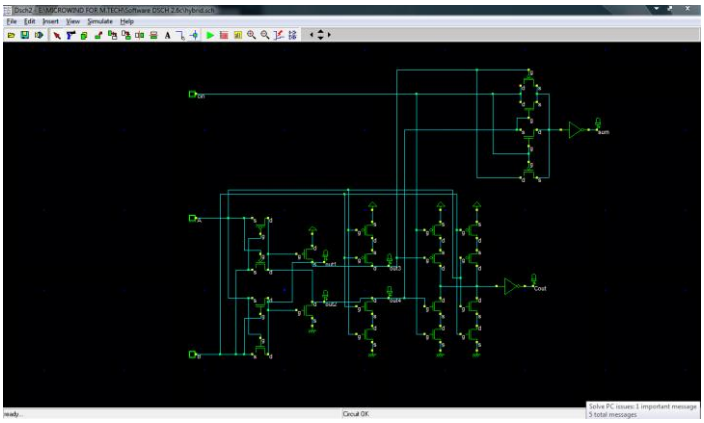


Fig.1.10. DSCH Schematic of Hybrid full adder

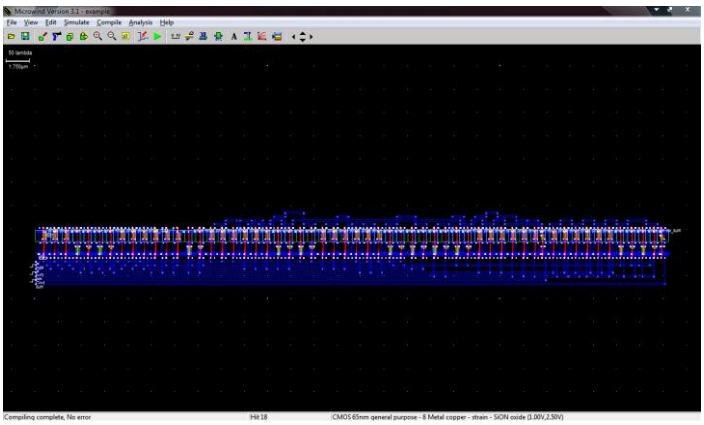


Fig.1.11 MICROWIND Schematic of Hybrid full adder

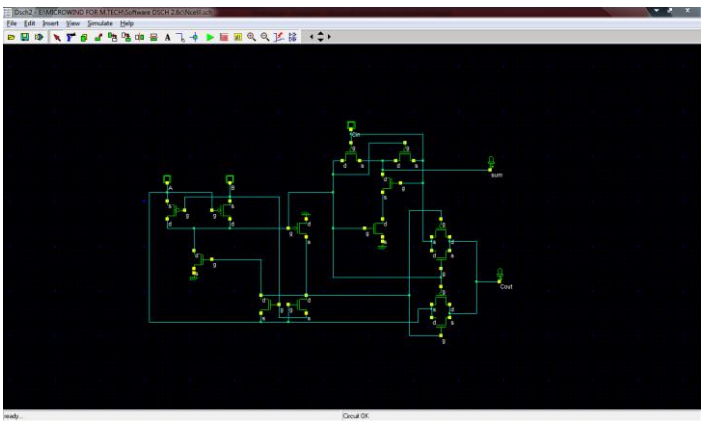


Fig.1.12 DSCH Schematic of NCell1 full adder

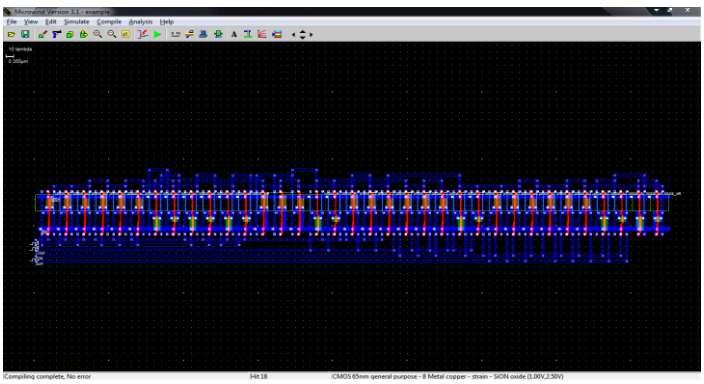


Fig.1.13. MICROWIND Schematic of NCell1 full adder

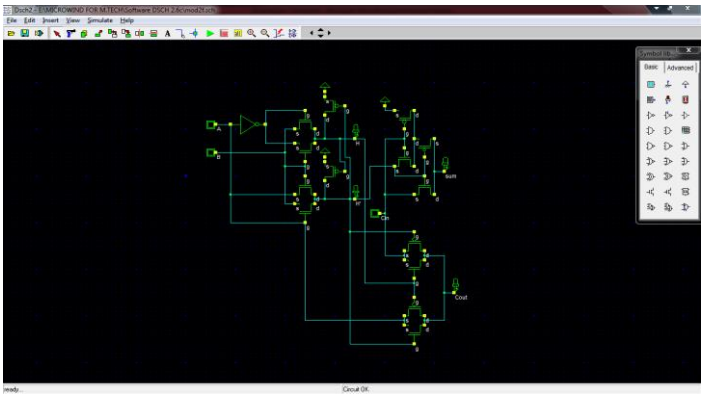


Fig.1.14. DSCH Schematic of Mod2F full adder

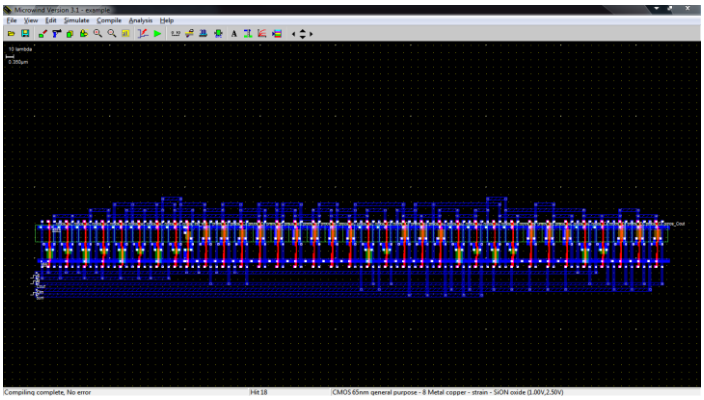


Fig.1.15 MICROWIND Schematic of Mod2F full adder

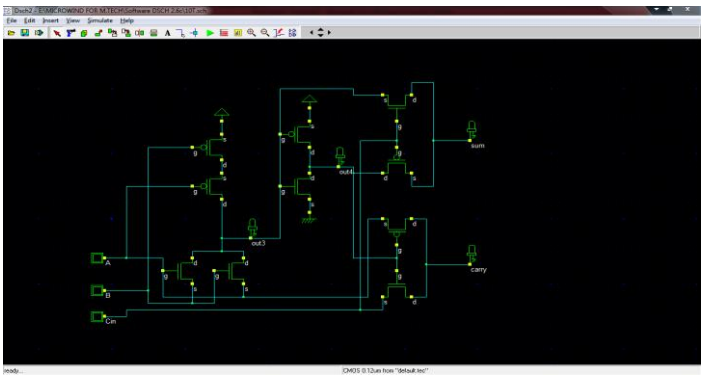


Fig .1.16. DSCH Schematic of N-10T full adder

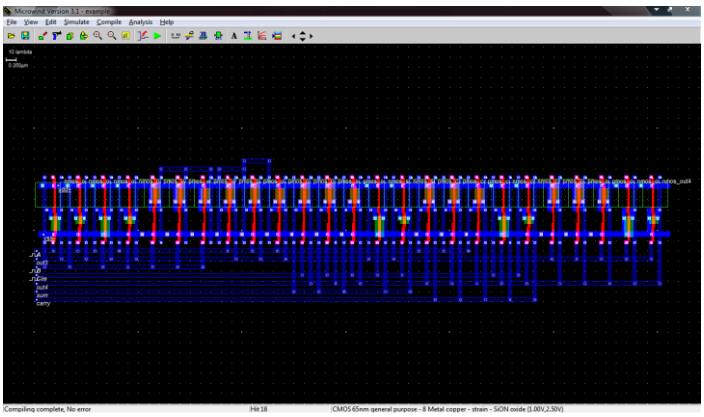


Fig.1.17. MICROWIND Schematic of N-10T full

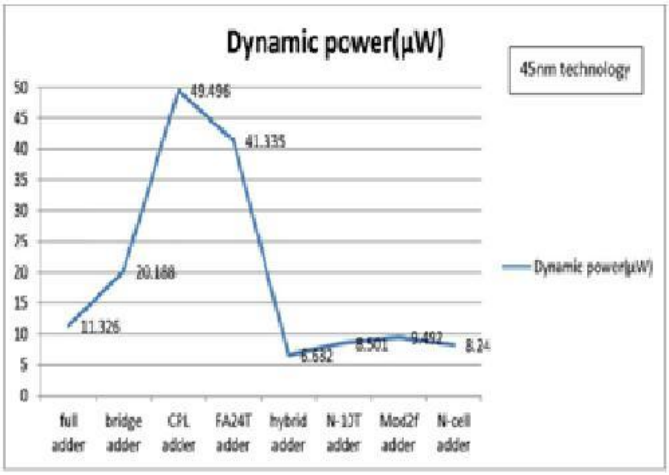
Fig [1.1]-[1.17] shows design of Conventional full adder, Bridge adder, CPL adder, FA24T adder, hybrid adder, N-10T adder, mod2f adder and N-cell adder using DSCH and MICROWIND software.

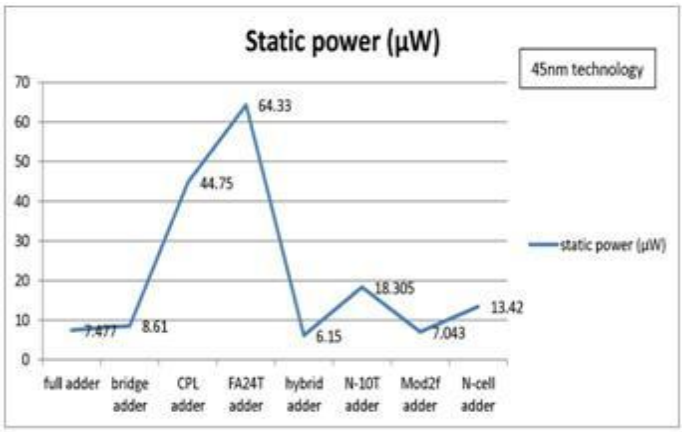
[9] DSCH is a logic editor and simulator which validates the architecture of the logic circuits and physical designing level is done in MICROWIND 3.1

III. FULL ADDER TESTING TABLES

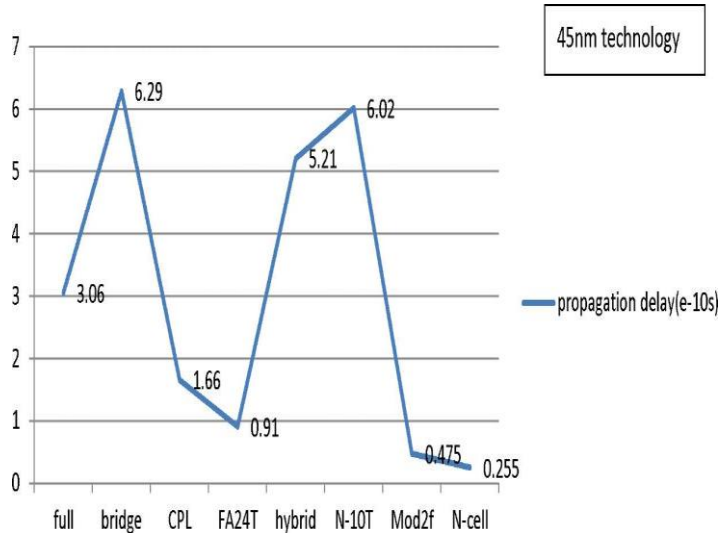
Now we will test all full adders using DSCH and MICROWIND software using three technologies namely 45nm, 65nm and 90nm in this section.

III.A ***Testing using 45nm Technology***

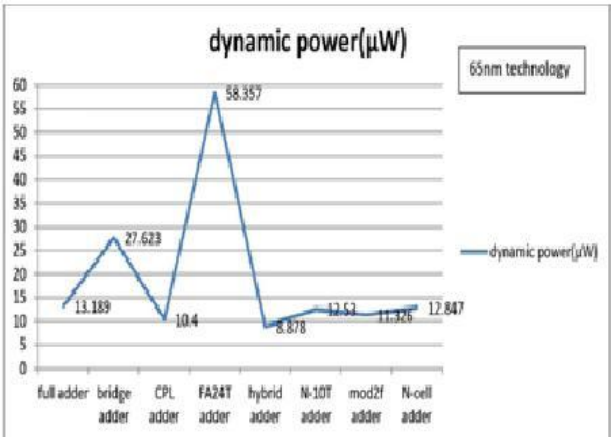


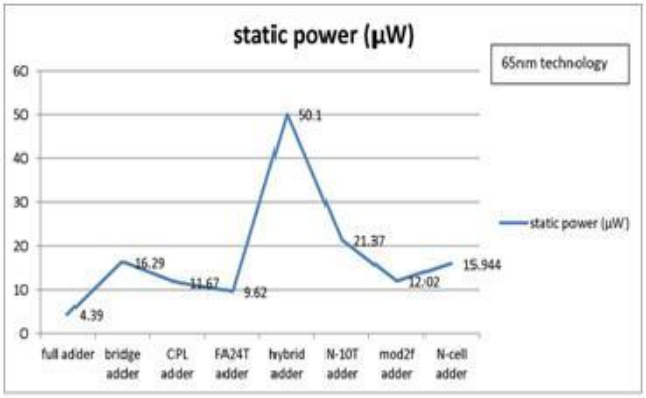


Propagation delay (e-10s)

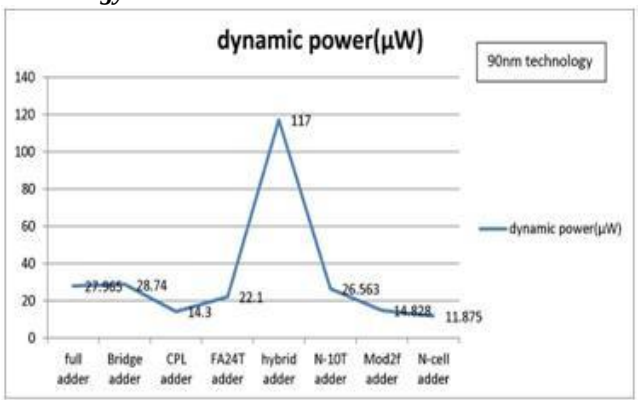


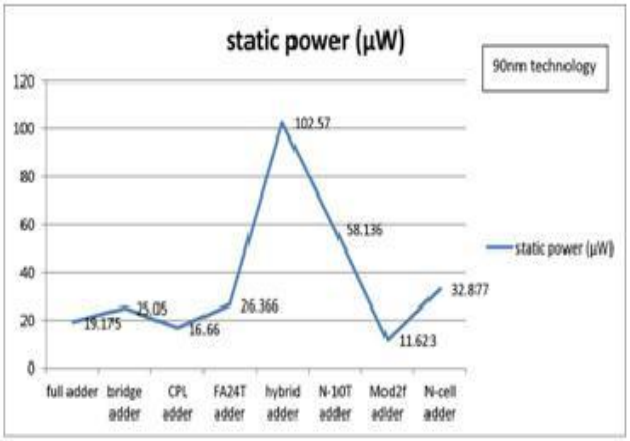
III.B ***Testing using 65nm Technology***

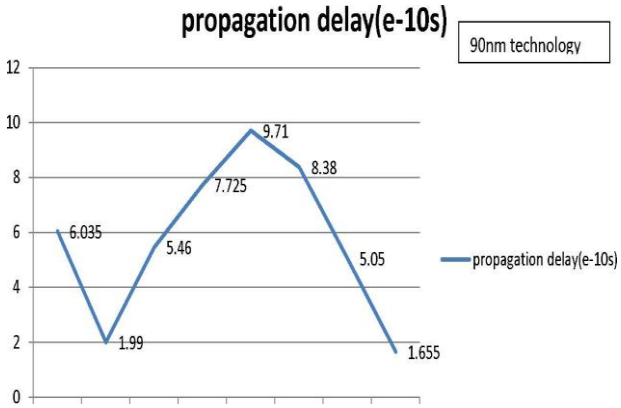




III.C ***Testing using 90nm Technology***







Full bridge CPL FA24T hybrid N-10T Mod2f N-cell

From testing graphs III.A, III.B and III.C there is clear cut trade-off between $P_{dynamic}$ and P_{static} as we decrease the technology that is 90nm, 65nm and 45nm in the presented paper. As we know that the total power dissipation P_{total} is equal to the sum of power dissipation during turn-off or P_{static} and power dissipation during turn-on or $P_{dynamic.}$ The P_{static} leakage is due to subthreshold leakage current [4] or drain to source current when the transistor is in OFF state. In this state since the V_{gs} is less than the threshold V_{th} the current flow is only due to minority carriers in the channels in the weak inversion mode. On decreasing the technology the channel length and channel width thus get reduced proportionally because of which the subthreshold conduction current (I_{sub}) increases. Thus increasing the static power dissipation.

The $P_{dynamic}$ on the other hand is decrease on decreasing the technology. Since on reducing the technology leads to effective reduction in the channel length the V_{th} that is the threshold voltage decreases because of which there is low leakage and better conduction which is due to majority carrier.
There is improvement in propagation delay due to shortening of channel length the carrier find easy path for travel. In general with reduction in technology there is substantial reduction dynamic power with increased static power. The propagation delay reduces drastically.

The paper present different full adder cells implemented in this three technology viz. 90nm, 65nm and 45nm. This also gives that with reduction in the number of transistor there is substantial improvement in the static and dynamics power dissipation. This different full adder cell with different transistor number was also implemented in this three technology and power dissipation was analyzed. The propagation delay was also analyzed and shows a clear trade-offs.

IV. CONCLUSSION

In this paper, 45nm, 65nm and 90nm technologies using DSCH and MICROWIND software has been presented. All three technologies were implemented in various full adder cells and it can be concluded that as we reduce the technology of the full adder cells the dynamic power though reduces, but its static power increases. Thus, we can recommend appropriate technology for particular application.

TABLE 1: MOS MODEL PARAMETERS

Parameters	Typical value of 0.45µm	
	nMOS	pMOS
V_{TO}	0.4V	-0.4V
U_O	$0.06m^2/V\text{-}s$	$0.06m^2/V\text{-}s$
T_{OX}	2nm	2nm
P_{HI}	0.3V	0.3V
GAMMA	$0.4V^{-0.5}$	$0.4V^{-0.5}$
W	1µm	1µm
L	0.12µm	0.12µm

NOMENCLATURE

V_{TO}	Threshold voltage (V)
U_O	Carrier Mobility (m^2/V-s)
T_{OX}	Gate oxide thickness (nm)
P_{HI}	Surface potential at strong inversion (V)
GAMMA	Bulk threshold parameter (V)
W	MOS channel width (µm)
L	MOS channel length (µm)

ACKNOWLEDGEMENT

First I would like to express my gratitude to Assistant Professor Manish Kumar my supervisor under whose guidance I have learnt low power and high performance full adder in deep submicron technology using 45nm, 65nm and 90nm technology and completed my project. He guided me wholeheartedly throughout the course.

I would like to express my gratitude to Dr. Rupaban Subadar, HOD Electronics and Communication Department and other faculties for their support and assistance.

Finally, I would like to thank my parents for their support, encouragement and providing me with all kinds of facilities I needed, to ensure that there are no hurdles in my work during tough times.

REFERENCE

[1]. Leakage Current Mechanisms and Leakage Reduction Techniques in Deep Submicrometer CMOS Circuits. Kaushik Roy, fellow, IEEE, Saibal Mukhopadhyay, student member, IEEE, and Hamid mahmoodi-meimand, student member, IEE.

[2]. Survey and evaluation of low-power full-adder cells Ahmed Sayed and Hussain Al-Asaad Department of Electrical & Computer Engineering University of California Davis, U.S.A.

[3]. Analysis of Subthreshold Leakage Reduction in CMOS Digital Circuits B.S. Deepak subramanyan and Adrian Nu˜nez EECS Department, Syracuse University Syracuse, New York 13244, U.S.A.

[4]. Two New Low-Power and High-Performance Full Adders by Mohammad Hossein Moaiyeri and Reza Faghih Mirzaee, Department of Computer Engineering, Science and Research Branch of Islamic Azad University, Tehran, Iran.

[5]. Low Power Full Adder Using 8T Structure Amin Bazzazi, *Member, IAENG,* Alireza Mahini and Jelveh Jelini.

[6]. Md. Asif Jahangir Chowdhury, Md. Shahriar Rizwan, and M. S. Islam 2012

[7]. Low Leakage SRAM design using sleep transistor stacks Abhishek Mathur, Arun Jayachandran, and Ramya Venumbaka CMOS Circuit Design, Layout, and Simulation Third Edition by R. Jacob Baker.

[8]. MICROWIND 3.1 and DSCH user manual lite version by Etienne Sicard.

[9]. www.microwind.org