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Research Paper

Bridgeless Sepic Converter for Renewable Energy Applications Using Matlab/Simulink

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ABSTRACT:- In present scenario the renewable energy become the most wanted sources for power production, for this power electronics plays a major role for the design of converters & Inverters, here in this paper focused on special type of inverter called sepic converter which is an advantage of boost and buck converters. In the proposed converter, the input bridge diode is removed and the conduction loss is reduced. In addition, the input current ripple is significantly reduced by utilizing an additional winding of the input inductor and an auxiliary capacitor. Similar to the conventional PFC SEPIC converter, the input current in a switching period is proportional to the input voltage and near unity power is achieved.

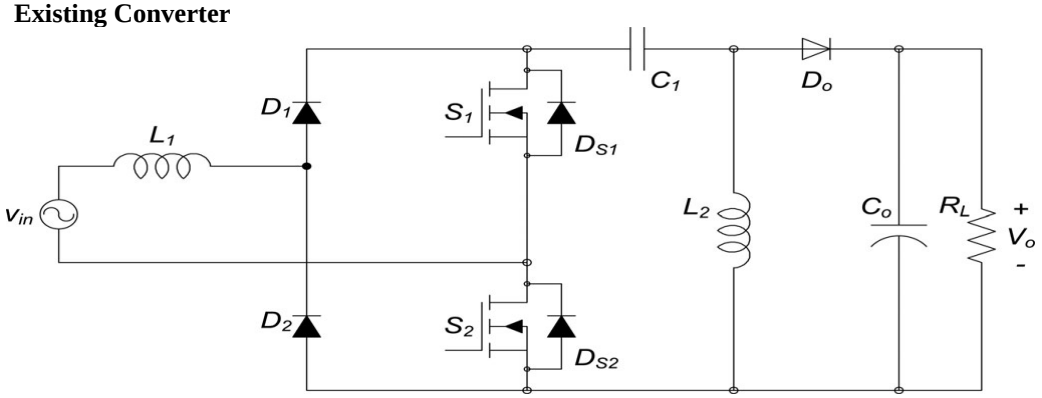
Keywords:- High output, Input ripple current, Power factor correction, Reduced harmonic losses, Sepicconverter,

I. INTRODUCTION

According to the demand on high efficiency and low harmonic pollution, the active power factor correction (PFC) circuits are commonly employed in ac–dc converters and switched-mode power supplies. Generally, these kinds of converters a full-bridge diode rectifier on an input current path so that conduction losses on the full-bridge diode occur and it will be worse especially at the low line. To overcome this problem, bridgeless converters have recently been introduced to reduce or eliminate the full-bridge rectifier, and hence their conduction losses .A bridgeless boost converter is widely used in advantages of reduced input current ripple, but its output voltage should be higher than the peak voltage of the input voltage. Relatively low output voltage of PFC converters is required in many applications such as low-voltage switched-mode power supplies.PFC buck converters are more suitable for these applications due to their low output voltage. A bridgeless buck converter was proposed like conventional PFC. buck converters, the output voltage of the converter proposed is lower than the peak value of the input voltage.

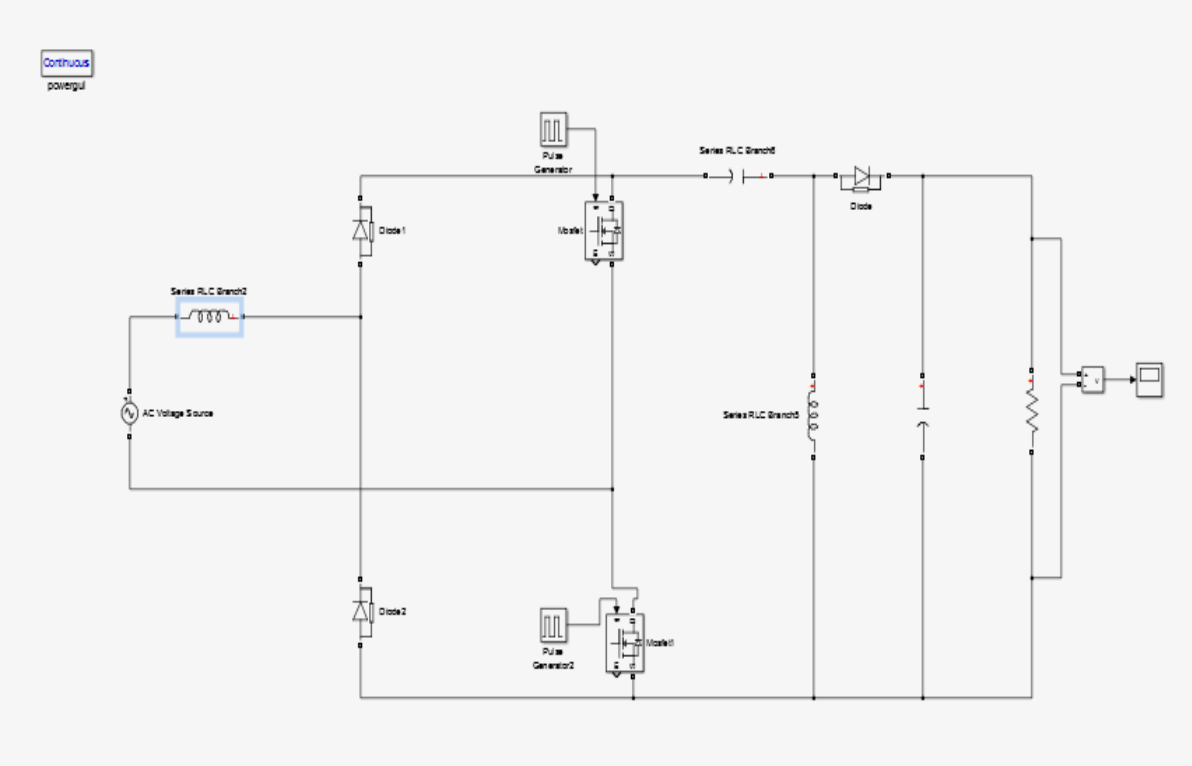
II. RESEARCH WORK ON EXISTING AND PROPOSED CONVERTERS

A. Existing Converter



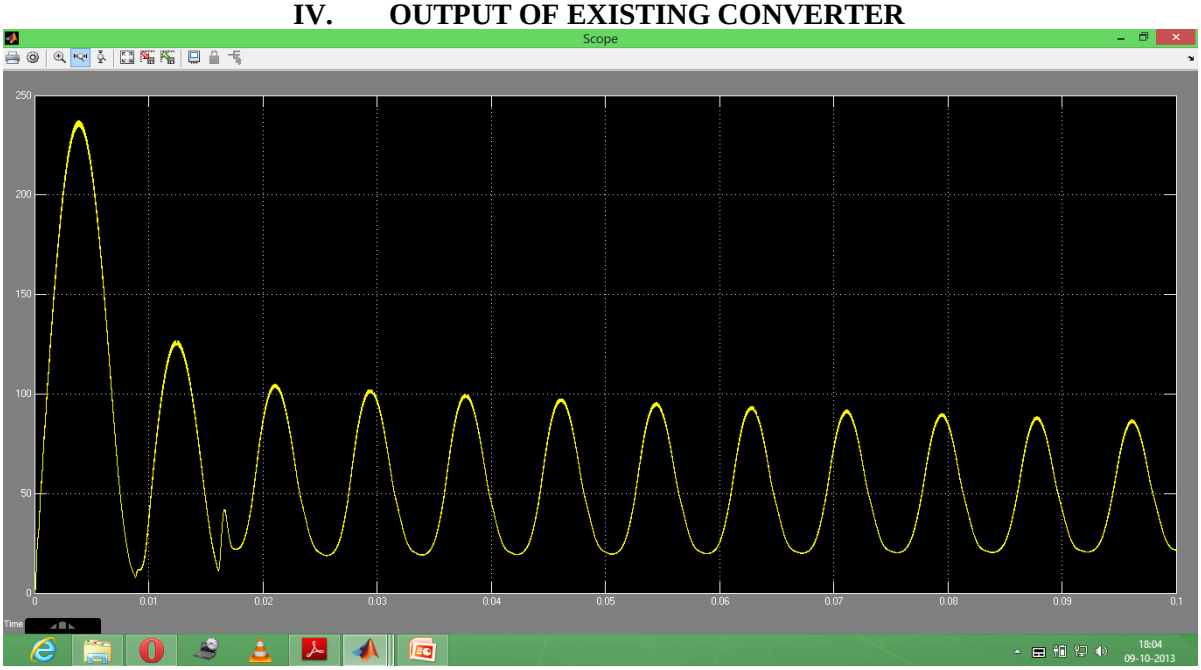
Conventional power factor correction (PFC) single ended primary inductor converter (SEPIC) suffers from high conduction loss at the input bridge diode. These kinds of converters include a full-bridge diode rectifier on an input current path so that conduction losses on the full-bridge diode occur and it will be worse especially at the low line. Suffers from high conduction loss at the bridge diode. The conduction loss is worse at the low line on the full bridge diode. Due to the bridge diode input ripple current will not be reduced.

III. SIMULINK MODEL OF EXISTING CONVERTER



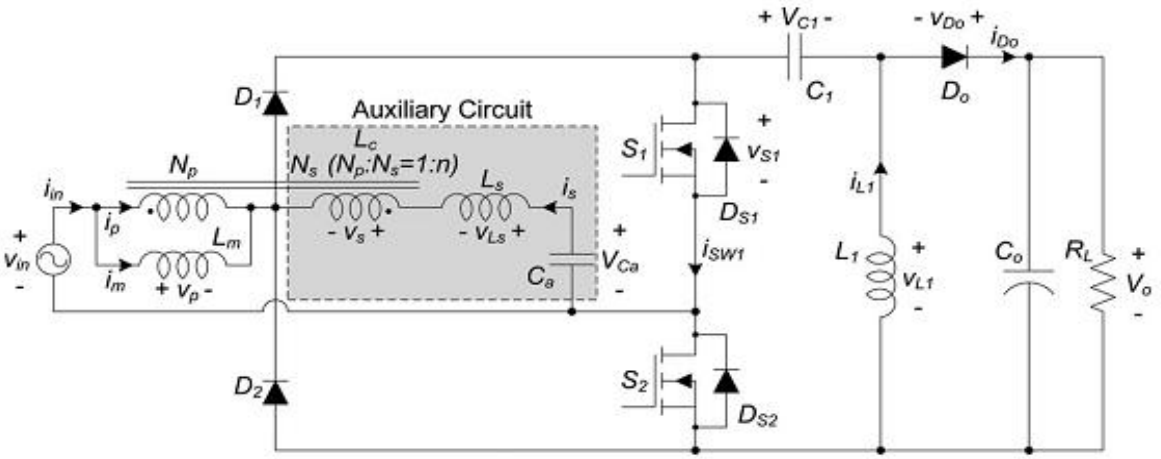
In the existing system due to the input ripple current, the ripple in the output voltage waveform is shown clearly.

IV. OUTPUT OF EXISTING CONVERTER



By observing the above figure it is very clear that there are lot of noises and distortions in the input side as well as output side, we are not getting the desired level of output as per the power electronics concern lot of harmonic distortions will occur in the output side the existing system has that disadvantage by verifying in the Simulink in order to eradicate that the proposed system is developed here.

V. PROPOSED CONVERTER



To solve this problem, a bridgeless SEPIC converter with input current is proposed. To overcome this problem, bridgeless converters have recently been introduced to reduce or eliminate the full-bridge rectifiers. A bridgeless boost converter is widely used in advantages of reduced input current ripple, but its output voltage should be higher than the peak voltage of the input voltage, and hence their conduction losses. An auxiliary circuit, which consists of an additional winding of the input inductor, an auxiliary small inductor, and a capacitor, is utilized to reduce the input current ripple. Coupled inductors are often used to reduce current ripple. It represents the auxiliary circuit for achieving the input current ripple cancellation. In figure shows the proposed gate signals for the switches. For a half period of the input voltage, one switch is continuously turned ON and the current via an intrinsic body diode is forced to flow through the channel of the switch. It can reduce the conduction loss on the switch further and the efficiency can be improved. For a better understanding we can see the various modes of operation in detail in the below chapters.

The output of an ideal SEPIC converter is:

$$Vo= D*V_i/1-D \qquad (1)$$

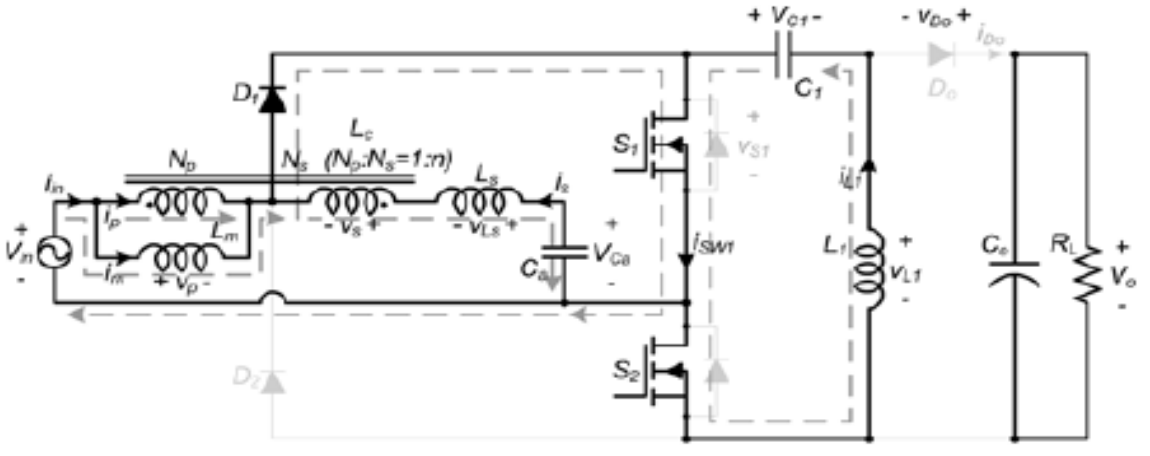
Vo = output voltage

D=Duty cycle

Vi= input voltage

VI. VARIOUS MODES OF OPERATION OF PROPOSED CONVERTER

A.MODE - I

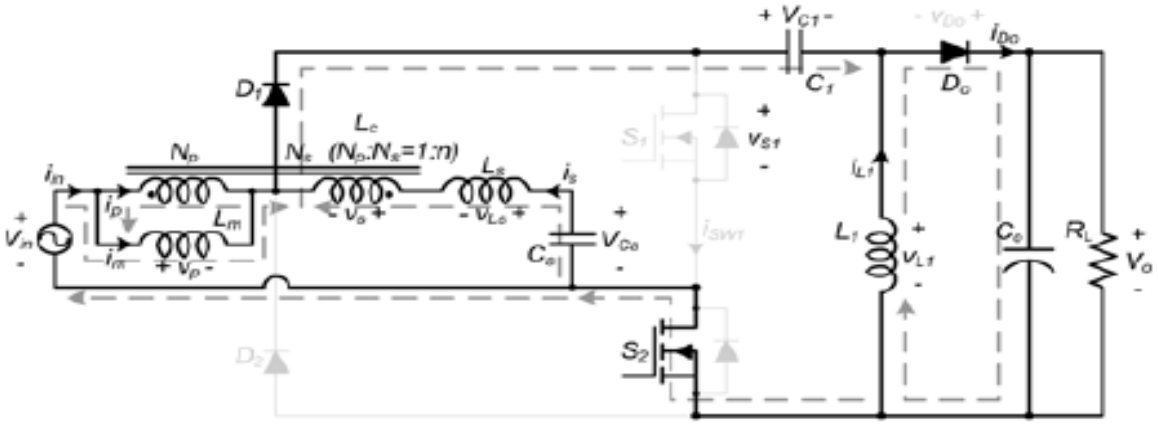


Mode 1

Mode 1 [t0, t1]: At t0, the switch S1 is turned ON and the switch S2 is still conducting. Since the voltage Vp across Lm is Vin, the magnetizing current increases from its minimum value Im2 linearly with a slope of Vin /Lm as follows:

$$i_s(t) = -I_{s2} + \frac{(1-n)V_{\text{in}}}{L_s}(t - t_0). \qquad (2)$$

B. MODE – II



Mode 2

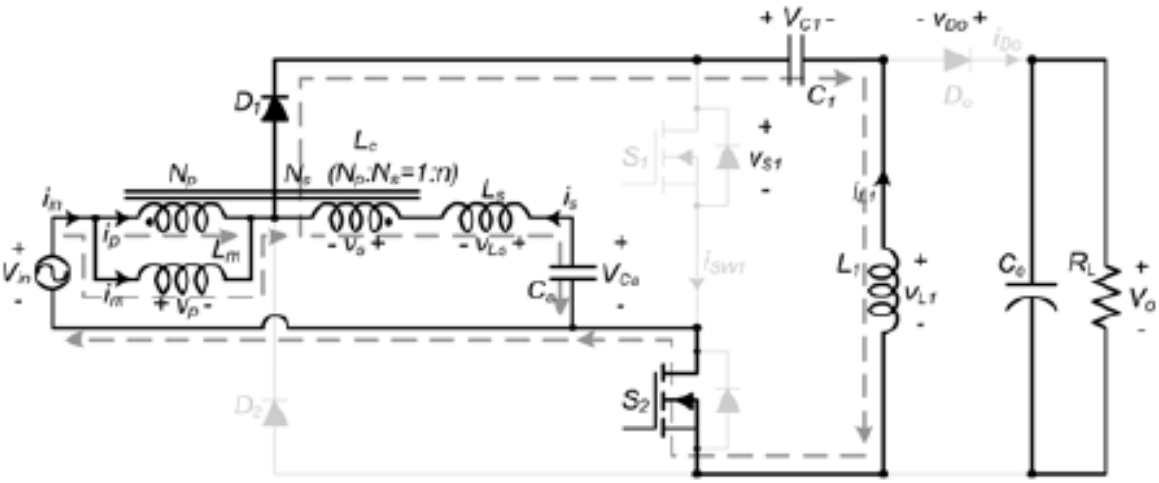
Mode 2 [t1, t2]: At t1, the switch S1 is turned OFF and the switch S2 is still conducting. Since the voltage Vpacross Lm is −Vo, the magnetizing current decreases from its maximum value Im1 linearly with a slope of −Vo /Lm as follows:

$$i_s(t) = I_{s1} - \frac{(1-n)V_o}{L_s}(t - t_1).$$

C. MODE – III

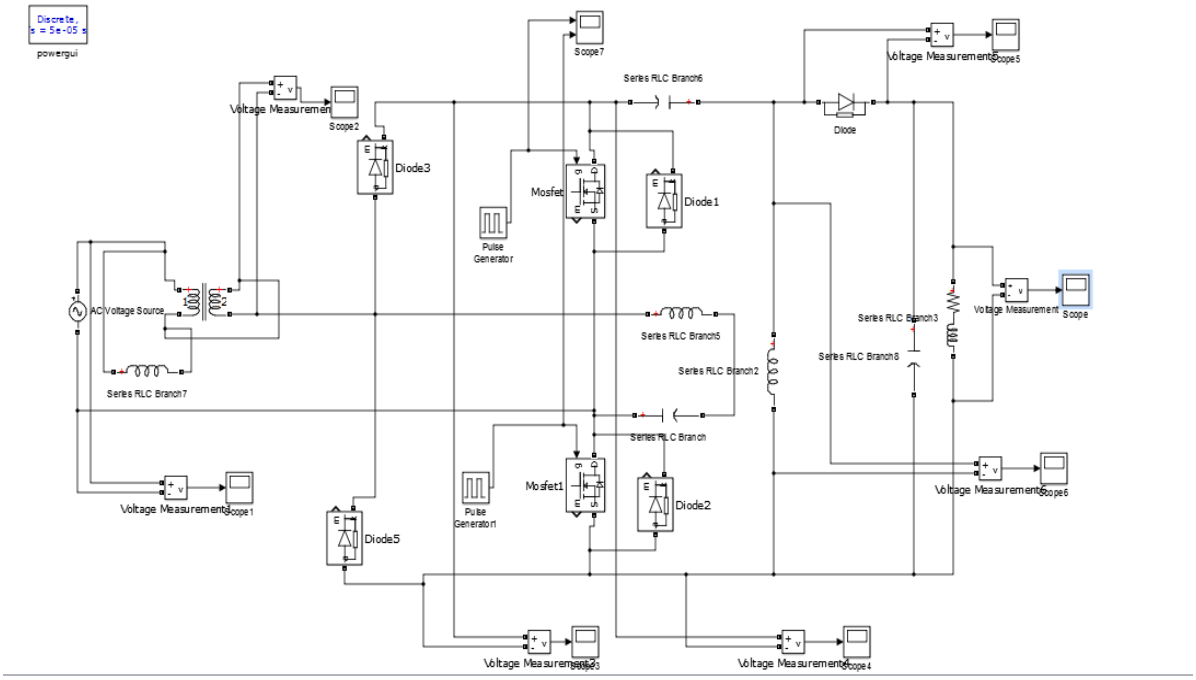
Mode 3 [t2, t0]: At t2 , the current iDo becomes zero, and the diode Do is turned OFF.
Since iin = im − nis = −is − iL 1 in this mode, the input current iin is the sum of freewheeling currents Is2 and IL2 as follows:

Iin = Im2 + nIs2 = Is2 + IL2 .

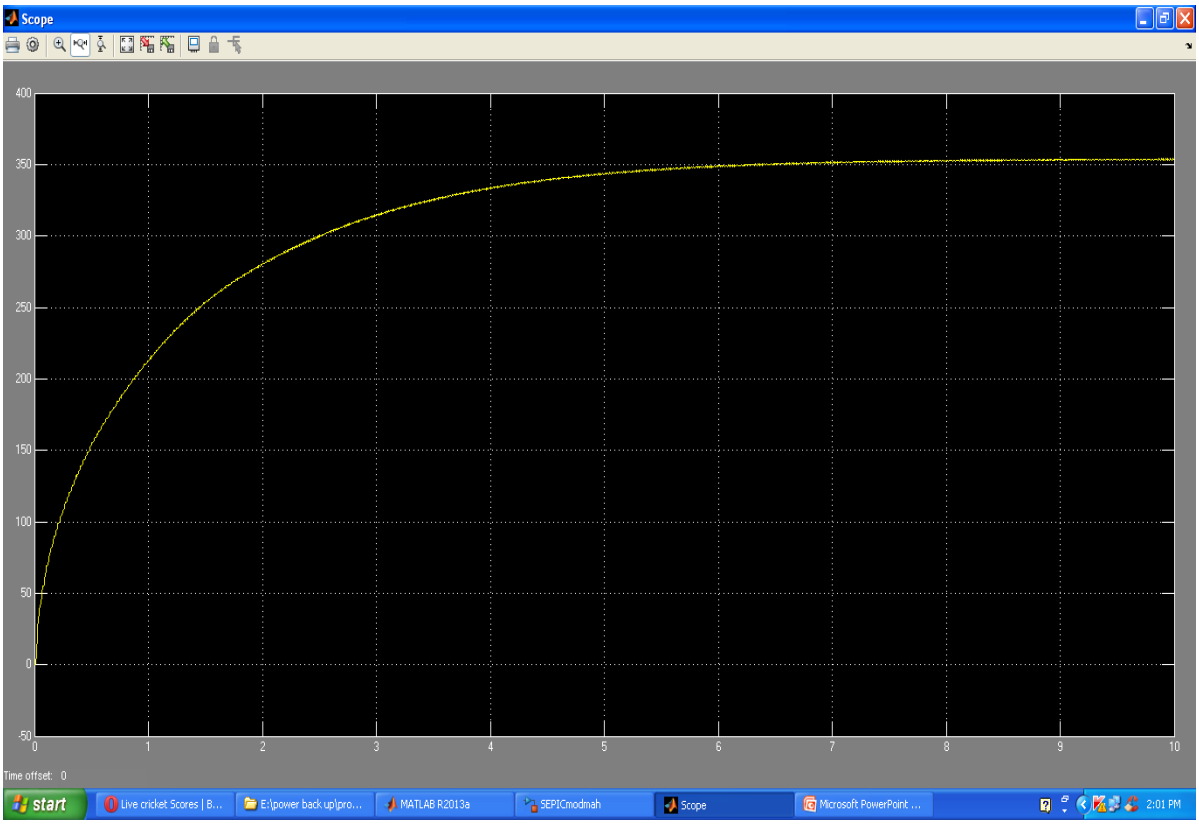


Mode 3

VII. SIMULINK MODEL OF PROPOSED CONVERTER



VIII. OUTPUT OF PROPOSED CONVERTER



IX. DESIGN SPECIFICATIONS

Design specifications of the proposed converter are as follows:

1) Main voltage range: Vin = 90 Vac –130 Vac ;
2) Line frequency: Fl = 60 Hz;
3) DC output voltage: Vo = 100 V;

4) Maximum output power: Pout = 130 W;
5) Maximum 2Fl output ripple: Δvo = 6Vpeak-peak ;
6) Switching frequency: fsw = 100 kHz.

X. CONCLUSION

A bridgeless SEPIC converter with ripple-free input current has been proposed. In order to improve the efficiency, the input full-bridge diode is eliminated. With the proposed gate driving method, the efficiency is improved by 0.45%. Input ripple current is minimized. To reduce the full bridge converter to bridgeless converter and hence reduces the conduction losses, Output voltage is very high. Some of the applications where this proposed converter is used are High power application, HVDC, Industrial application, DC-Drives. Finally the SEPIC converter is an advanced converter which has the advantages when compared to buck and boost converters.

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