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Research Paper

Design and implementation of low power 4-bit ALU using adiabatic logic based on FinFET technology

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Abstract
With the relentless growth of device technology, leakage power has become the most consequential source of power consumption, reducing the energy recovery efficiency of adiabatic logic by a large extent. In this study, a unique low-power adiabatic logic based on FinFET devices has been suggested. All microprocessors have an ALU at their core. ALUs are becoming more intricate and smaller in size these days, making an allowance for the advent of smaller, more powerful computer systems. An ALU is a combinational digital electrical circuit that serves as the CPU's core. Three arithmetic and four logical operations are performed by the 4-bit ALU architecture. ADD, SUBTRACT, and COMPARE are the three arithmetic operations. AND, OR, XOR, and NOT are the four logical operations. Power gated adiabatic inverter circuits employing techniques like ECRL have additionally been constructed to validate the proposed approach. Due to the fact that FinFET has lower threshold voltages than adiabatic logic, it is feasible to implement adiabatic logic FinFET based ALU at lower operating voltages.

Keywords: *FinFET,4-Bit ALU, Adiabatic Logic, ECRL*

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I. INTRODUCTION

MOS (Metal Oxide Semiconductor) transistors have played a critical role in improving the performance of integrated devices thanks to integrated chip technology, which has transformed the world of electronics. MOS devices have been continually scaled over the last two decades in order to reach high density and performance. Planar double gate FETs and FinFETs have become a potential new solution for low power digital CMOS advancements. Due to the difficulty in lowering the size of standard bulk transistors, a novel device architecture was developed in which each device has two gates, one on each side of the body. Although early double gate devices had manufacturing issues due to their vertical construction, as of late, double-gate devices such as FinFET or wrap around FETs that are viable with customary CMOS have been developed. FinFETs have particular benefits when it comes to scaling to extremely short gate lengths. FinFET fabrication is comparable to that of ordinary MOSFETs, although it is closer to that of SOI devices.

Individual device scalability has its limits, and as process technologies shrank closer to 20 nm, it became hard to accomplish correct scaling of various device parameters. One of the most important factors which was especially affected was the power supply voltage. Optimising for one aspect, such as performance, led to unintended trade-offs in other areas, such as power. As a result, additional, more innovative possibilities, such as a shift in transistor structure from the typical planar transistor, have to be considered.

One of the major concerns is that as technology advances, the source and drain of the MOS devices utilised encroach into the channel, making it easier for leakage current to pass between them and making it impossible to completely switch the transistor off. Short channel phenomena such as Vt roll-off and drain-induced barrier lowering will take place when scaling standard CMOS devices down. Increase in leakage current, sub-threshold leakage, gate direct tunnelling leakage, and hot carrier effects are additional concerns.

Increased power consumption is caused by gate leakage. Inverter power consumption, for example, is related to gate switching frequency, total load capacitance, and gate switching fraction. The substrate and oxide current leaking influence the leakage current. Because the charging and discharging of CL occurs with greater magnitude than CMOS due to the suppression of leakage current, the problem of dynamic power is alleviated when utilising FinFET devices. To address these difficulties, a novel device paradigm for processing element design based on FinFET technology has been presented. FinFET technology carries the advantages of higher drain current and switching speed, along with reduced static leakage current.

The static CMOS logic is the most well-known and reliable, although it has a significant drawback of leakage current and poor performance. Dynamic logic is a high-performance circuit with minimal power dissipation, but its resilience suffers as a result. Subthreshold logic uses a supply voltage VDD that is lower than the transistor's threshold. In the saturation region, CMOS logic uses more power than the identical logic operating in the subthreshold area. To reduce dynamic power consumption, adiabatic logic with robust inversion and noise immunity can be employed.

II. LITERATURE SURVEY

B.G. Kumar et al. [1] proposes that FinFETs are superior to CMOS, in terms of voltage, area and power. The fin that wraps around the channel of a FinFET gives electrical control. The gate in CMOS devices loses channel control, resulting in higher leakage current, parameter fluctuations, worse reliability, yield, and short channel effects. The most often utilised memory cell for preserving data until the power supply is activated is the Static Random-Access Memory [SRAM] cell. The primary aim is optimizing the power and delay constraints of the SRAM cell. Both FinFET technology, as well as adiabatic logic has been used to meet the required conditions.

Utkarsh Tripathi et al. [2] devised an adder circuit including a full adder CMOS circuit and it is developed utilising MOSFETs with a length of 32nm and in FinFETs with 28 transistors in MOSFET and FinFET. Then, a HSPICE software simulation is done and the adder's performance characteristics, such as average power and delay are determined in both FinFET and MOSFET counterparts. Thus, in conclusion, FINFET provided the best results in terms of average power consumption and delay. DGFETs have emerged as a potential way to keep the process going. FinFET has emerged as a leader among DGFETs where scaling up of technology is concerned. They remain the most pragmatic option due to the ease of manufacture.

The significant short channel effects that produce an exponential rise in the leakage current and increased susceptibility to changes during the process make scaling of ordinary single-gate bulk MOSFETs difficult in the nanoscale realm. Multi-gate MOSFETs overcome these drawbacks by allowing for more precise control over a thin silicon body with many electrically connected gates. The double-gate FinFET is the most suitable of the multi-gate transistor topologies due to the self-alignment of the two gates and the familiarity of the manufacturing procedures with current standard CMOS technology.

A. Raghunandan uses FinFET based adiabatic logic circuits to design logic gate such as buffers, XOR/XNOR, and AND/NAND circuits. The circuits have been designed using FinFET 18nm technology. The average power of the circuits, as well as the output energy loss of the circuits were determined. For the Buffer, the average power consumption was found to be 4.331uW without adiabatic logic and 1.840uW with adiabatic logic. The reduction of power is 57.51%. For the AND/NAND circuit, average power consumption was found to be 4.479uW without adiabatic logic, and 2.356uW with adiabatic logic. The reduction of power is 47.39 % For the XOR/XNOR circuit average power consumption was found to be 7.778uW without adiabatic logic and 4.428uW with adiabatic logic. The reduction of power is 43.07 %. The energy loss is reduced from 8.74 % to 8.12%.

Jayashree K.G. et al. [4] has proposed an energy efficient and novel Charge Sharing Complementary Pass Transistor Adiabatic Logic (CSCPAL), operated by a four-phase power clock. It realizes low switching noise and incurs low leakage power. The circuits were designed using 32nm FinFET models and were simulated using Cadence Virtuoso design tools. By comparing it to current FinFET-based 2N2N2P, 2N2P, and PFAL circuit analogues, the efficiency of the proposed CSCPAL circuit is proven.

CSCPAL's average energy usage is compared to 2N2N2P, 2N2P, and PFAL. The design of the 8-bit CLA architecture validates the efficiency of CSCPAL. In addition, the energy efficiency of the XOR and AND logic blocks employed in the CLA design is examined. FinFET based CSCPAL inverter circuit is 41%, 35% and 52% more efficient than FinFET based 2N2N2P, 2N2P and PFAL circuits, respectively.

Mayank Shrivastava et al. [5] goes over the process features of the proposed device.

A thorough 3-D device/mixed-mode simulation provides physical insight into the improvement in short-channel performance and power dissipation. Detailed electro-thermal simulations are used to compare the proposed device's self-heating behaviour to that of regular FinFETs. The suggested device necessitates an

additional production step, but it allows for a lower electrical width in self-loaded circuits, making it a great choice for SoC applications.

Shivani Chopra et al. [6] presents an outline of the challenges that arise when MOS devices are downscaled. Scaling issues such as power supply and threshold voltage scaling, gate oxide tunnelling, random doping fluctuation, high electric field, source to drain tunnelling, and short-channel effect should all be well understood in order to maintain device density growth. Adopting standards based on nanostructures at the molecular level ones might be a way for the microelectronics industry to keep up with the high-density pace.

Scaling of CMOS technology has been a critical component of the silicon-based semiconductor industry's continued success. Moore's Law, which gave basic criteria for transistor design to enhance circuit density and speed, has been followed by scaling for a few decades. Because more transistors can be put on a single chip, greater circuit performance and density enable more sophisticated functionality. However, as device scaling continues into the twenty-first century, it becomes clear that Moore's Law's historical growth, doubling circuit density, and higher performance cannot be sustained only by traditional scaling theory. Increased leakage current hinders further threshold voltage decrease, which in turn prevents supply voltage scaling for speed increase. Increased leakage currents and device reliability are harmed by higher electric fields generated inside the transistor. Furthermore, the high channel doping required poses substantial problems, including mobility degradation and threshold voltage variations caused by random dopants.

As device scaling approaches its physical size restrictions, many studies are being conducted to discover an alternate means to keep Moore's law alive. Due to rising power consumption, process variance, and fabrication costs, the technological cycle is slowing. Due to the current compromises between performance and power consumption in device scaling, technical advancements that can deliver great performance while consuming very little power are necessary.

Even if significant attempts are made to sustain sophisticated CMOS technology, it will not last more than a few decades. As a result, developing gadgets should be taken into account in order to keep up with technological advancements in the near and far future.

The quantity of power dissipated by VLSI circuits is one of today's significant challenges in circuit design. The technology of adiabatic logic is becoming a solution to the problem of power dissipation. The word "adiabatic" refers to a state shift that happens without losing or gaining heat. During switching events, the adiabatic switching approach decreases power consumption. Adiabatic circuits, on the other hand, are extremely dependent on power clock and parameter fluctuations. MUX, one bit sum and carry adder are developed and simulated on cadence Virtuoso utilising 180nm technology. When compared to the traditional CMOS design approach, the suggested technique exhibits a reduction in power dissipation. And the results show that adiabatic logic may be utilised to create reasonably big, sophisticated circuits that disperse much less heat than traditional CMOS designs.

Jitendra Kanungo et al. [8] examined the energy efficiency of a whole adiabatic system at the 90 nm CMOS technology node, incorporating the Power Clock Generator (PCG). In terms of energy efficiency, the PCG's conversion efficiency is thoroughly tested. In order to test the conversion efficiency of PCG, energy performance is extensively carried out by varying supply voltage and the driver transistor's width. The proposed PCG is used to drive the 4-bit adiabatic Ripple Carry Adder (RCA) and the obtained simulation results are compared with the adiabatic RCA driven by the reported PCG. The simulation findings are compared to the adiabatic RCA driven simulation results by the PCG that has been reported. In the clock, the suggested PCG has a maximum conversion efficiency of 56.48% across a frequency range of 25 MHz to 1GHz. The design of an efficient PCG boosts the energy savings of adiabatic logic, as seen in the study.

When compared to static CMOS, adiabatic logic circuits have a significantly lower power dissipation. A novel energy recovery logic is subthreshold adiabatic logic. The effectiveness of all logic gates using this unique logic is compared to its traditional equivalent in P. Kalyani et al. [9]. The performance and energy consumption of each logic gate circuit are investigated using various technologies, supply voltages, and operating frequencies. CADENCE technology is used to design and simulate the suggested circuits. In comparison to static CMOS, simulation studies demonstrate that subthreshold adiabatic logic saves more than 90% of power.

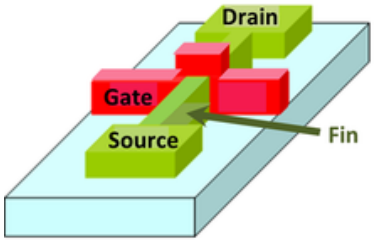
The numerous adiabatic logic families are discussed by Akash Agrawal et al. [10]. Different logic gates have been constructed for the new logic circuit utilising different logic families and suggested DCDB-PFAL logic at various frequencies and for various dc voltages. Finally, for both the proposed and traditional logic, a 2:1 MUX combinational circuit has been built. According to simulations of current logic families, the PFAL logic family has a substantially lower power dissipation than the ECRL and 2N- 2N2P logic families. And we can see from the simulations in this work that the suggested DCDB-PFAL logic circuits conserve a lot of power compared to other logic groups and have even better performance and lower power dissipation than the PFAL logic group.

Different figures show that as the dc voltage is changed between 0.1V and 0.3V, power declines at first until roughly 0.25V and then steadily increases. The suggested DCDB-PFAL logic can be utilised in medical

equipment that require very minimal power to operate, such as hearing aids, pacemakers, and other medical devices. As the need for ultra-low power circuit designs grows, these upgraded circuit technologies will be extremely valuable in meeting that demand.

III. FinFET TECHNOLOGY

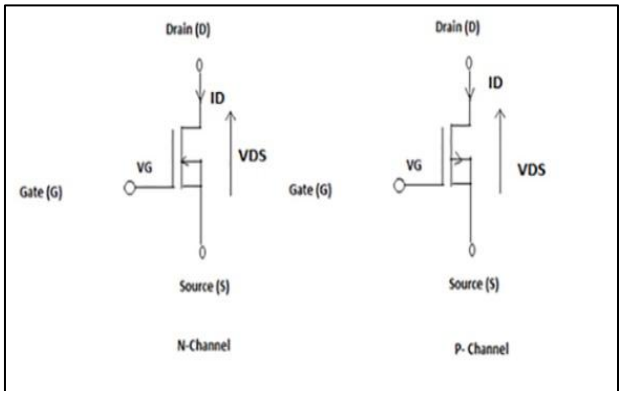
A fin field-effect transistor is a multi-gate device. It is a MOSFET built on a substrate where the gate is placed on two, three, or four sides of the channel or wrapped around the channel, forming a double or even multi-gate structure. These devices have been named "FinFETs" because the source/drain region forms fins on the silicon surface. The FinFET devices have faster switching times and higher current density than planar CMOS technology, by a significant amount. It is the basis for modern nano electronic semiconductor device fabrication.



Structure of FinFET

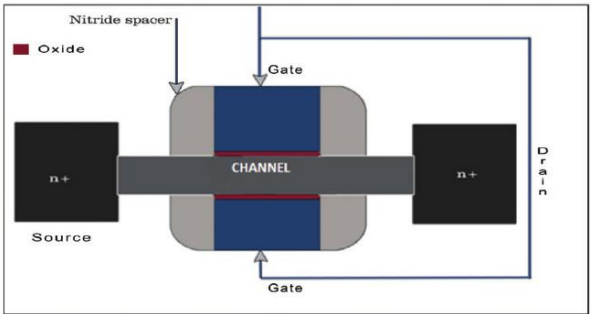
Working principle of FinFET

A FinFET's operating principle is similar to that of a regular MOSFET. For p-channel as well as n-channel MOSFETs, there are two modes of operation: enhancement and depletion. When there is no voltage on the gate terminal, the channel has the highest conductivity. The conductivity of the channel decreases when the voltage goes from positive to negative.



Depletion mode MOSFET

When there is no voltage on the gate terminal of a MOSFET in enhancement mode, it does not conduct. In contrast to depletion mode, the device conducts better in enhancement mode when the gate terminal voltage is higher. The MOSFET's primary function is to regulate the passage of voltage and current between the source and drain terminals. The gate terminal creates a high-quality capacitor. The silicon oxide layer, the p-body silicon, gate metallization, and the p-body silicon make up the gate. The most important component is the capacitor. The semiconductor surface lies under the oxide layer, between the source and drain terminals. By adding a positive or negative gate voltage, this is reversed from p-type to n-type. A depletion area is generated when a little amount of voltage is given to this structure (the capacitor) while keeping the gate terminal positive in relation to the source. At the contact between silicon and SiO2, this depletion zone forms. The source terminal, the drain terminal, and the n+ source all attract electrons when a positive voltage is supplied. The electron reach channel is created as a result of this. Current will flow between source and drain terminals if voltage is supplied between them. The gate voltage regulates the number of electrons in a circuit (Vg).



Cross-sectional view of FinFET

A hole channel will develop under the oxide layer if a negative voltage is supplied. Current conduction between the source and the drain is now controlled by the source to gate voltage. Only when the gate voltage passes a certain threshold does conduction commence.

Advantages of FinFET

1. Better command over the channel
2. Stifled short-channel impacts
3. Lower static leakage current
4. Lower switching voltage

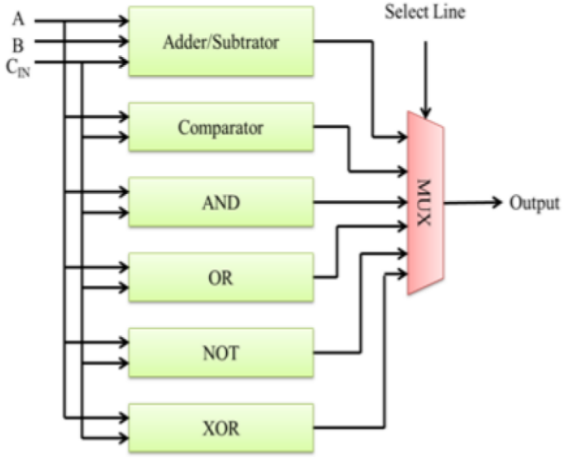
FinFET applications

i. Low power design in digital circuits, such as RAM, because of its low off-state current.
ii. Used in manufacturing microprocessors.
iii. Also finds its applications in home computers, laptops, tablets, smartphones, wearables, high-end networks, automotive, and more.

IV. PROPOSED SYSTEM

Overview:

In digital electronics, an arithmetic logic unit (ALU) is a digital circuit that performs arithmetic and bitwise logical operations on integer binary numbers. The designed ALU circuit performs addition/subtraction and comparator operations and even a few logic functions.



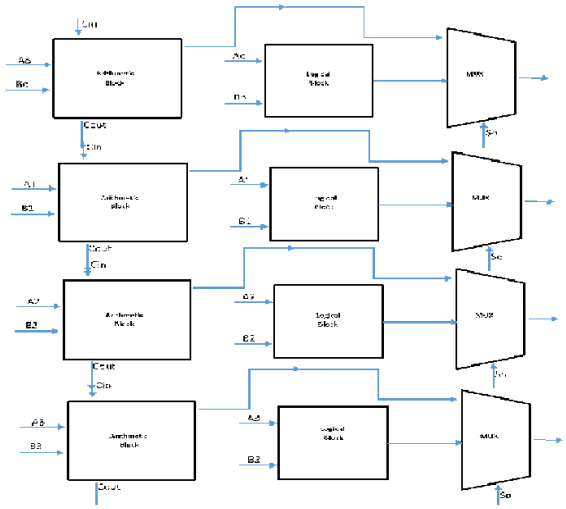
Block diagram of proposed ALU

As seen in the block diagram of the proposed ALU, the full adder/subtractor has three inputs so three inputs are taken namely, A, B and Cin. Apart from the adder/subtractor, the rest of the operations need only two inputs. The functions are selected by multiplexer with the select line and output is obtained.

Design of 4-bit ALU:

Four 1-bit ALU blocks are cascaded to create a 4-bit ALU. Each 1-bit ALU comprises of the following elements:

1. Arithmetic 4:1 multiplexer
2. Logical 4:1 multiplexer
3. 2:1 multiplexer to select either arithmetic or logic operation



Block diagram of 4-bit ALU

Each bit employs three multiplexers and one full adder. The 4:1 multiplexers have two select lines SO and SI. The MUXs provide the required input signal for the adder circuit depending on the operation being performed on the input signal, and also pass the output of the full adder to 2:1 multiplexer for further selection. The select line S2 is used for 2:1 MUX for selecting the arithmetic function (S2=O) and logical function (S2=1), as seen in the table below.

S2	S1	S0	Operation
0	0	0	Addition
0	0	1	Subtraction
0	1	0	Compare(A<B)
0	1	1	Compare(A>B)
1	0	0	AND
1	0	1	OR
1	1	0	EXOR
1	1	1	NOT

ALU operation

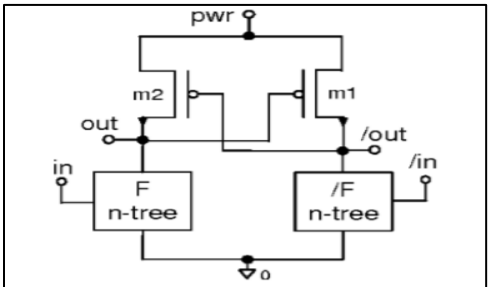
i. Arithmetic operations: Arithmetic is the most basic field of mathematics. It entails the investigation of numbers, particularly the characteristics of the classical operations of addition, subtraction, multiplication, and division. Arithmetic is a fundamental aspect of number theory, which, along with algebra, geometry, and analysis, is regarded one of the top-level divisions of modern mathematics. The developed arithmetic logic unit performs addition, subtraction, and comparison arithmetic operations. Lesser, greater, and equal operations make up the comparator.

ii. Logic operations: A logic gate is the fundamental component of a digital circuit which implements a Boolean function. A logical operation is performed on one or more binary inputs that produces a single binary output. Although digital logic gates can have several inputs, they usually only have one digital output. Individual logic gates can be combined to build larger logic gate functions, such as combinational or sequential circuits. AND, OR, NOT, and XOR are among the logic operations performed by the proposed ALU circuit. FinFETs have been used to replace every gate structure.

iii. Multiplexers: Multiplexers are devices that combine data from several sources into a single stream. The select lines allow the MUX to choose which input should be switched to an output. 2:1 MUX and 4:1 MUX were built and simulated in this study. Two inputs, one select line, and an output make up the 2:1 MUX. A 4:1 MUX has four inputs, two select lines, and one output.

iv. Validation using adiabatic approach: Adiabatic circuits are low-power circuits that conserve energy by using "reversible logic." Unlike typical circuits, which lose energy as they change, adiabatic circuits commit to charge conservation by following two simple rules: When there is a voltage potential between the supply and the drain, the transistor should never be activated. Once current is flowing through a semiconductor device, it should never be turned off. Full adders based on adiabatic logic have been developed, and they may be compared to XOR and XNOR based full adders.

Efficient Charge Recovery Logic (ECRL)
The logic of ECRL is made up of a pair of pull-down NMOS networks and pull-up PMOS networks. In this procedure, both pre-charge and assessment (evaluation) are done at the same time. It eliminates the usage of diodes, resulting in reduced energy dissipation. Because of the PMOS threshold voltage, it has a weak zero logic. As a result, the ECRL circuit has a smaller noise margin.

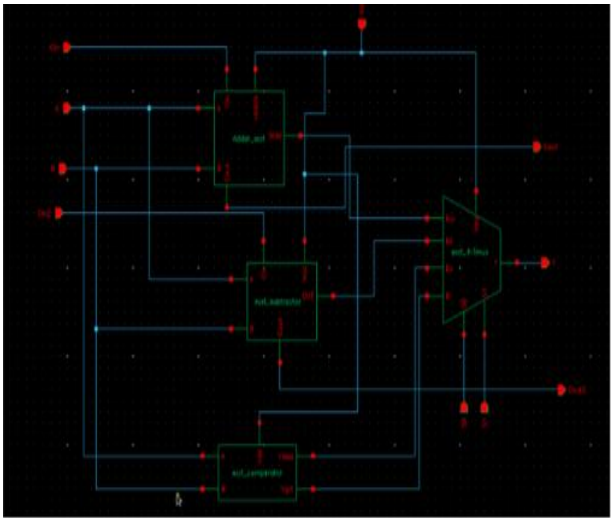


ECRL logic-based inverter circuit

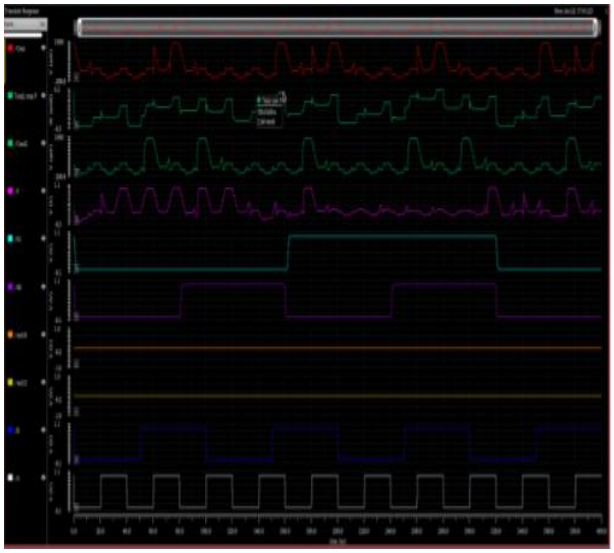
There are four stages to the power clock utilised in the adiabatic approach. They are:
(i) Evaluate (E) - In interval E, i.e., in the evaluation phase, the outputs get evaluated from the stable input signal.
(ii) Hold (H) - During interval H, i.e., the Hold phase, the output is kept stable to provide input to the next stage.
(iii) Recovery (R) - During interval R, i.e., the recovery phase, the energy gets recovered, and
(iv) Wait (W) - In interval W, i.e., the wait interval provides symmetry.

V. RESULTS AND DISCUSSION

Each 1-bit ALU has a logical and arithmetic block. The arithmetic block has a 4:1 MUX adder, subtractor, and comparator. The schematic of the arithmetic block and the output of the corresponding circuit is shown in the figures below.

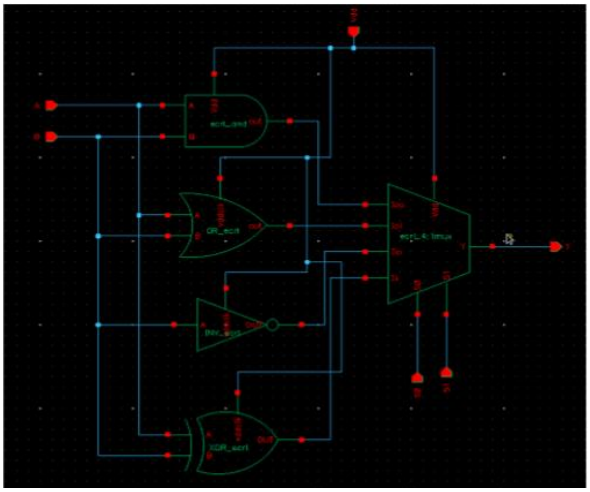


Design of arithmetic block

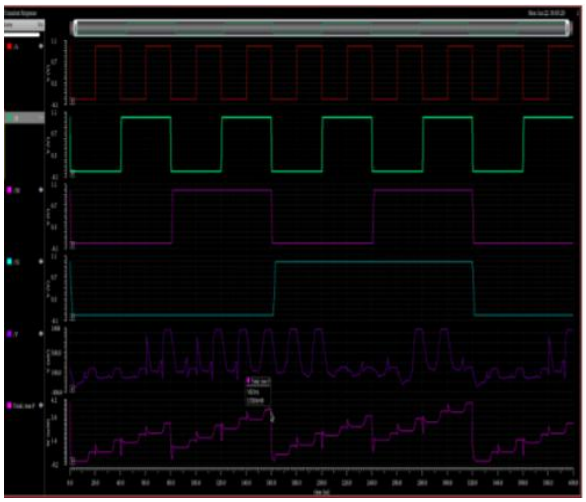


Simulation results of arithmetic block

AND, OR, NOT, and XOR operators are supplied to 4:1 mux in the logical block. The schematic of the logical block and the corresponding output are shown in the figures below.

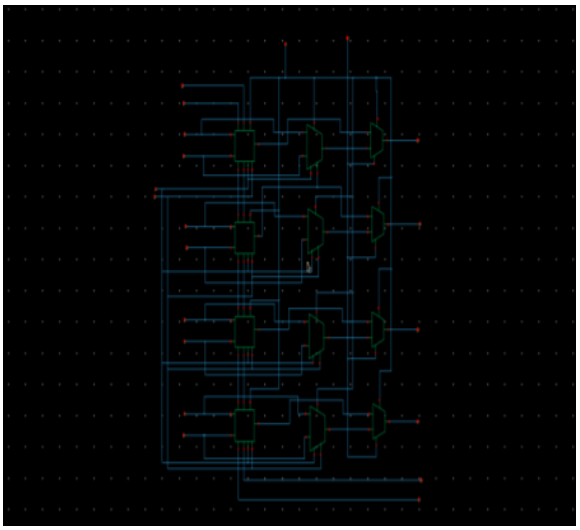


Design of logical block

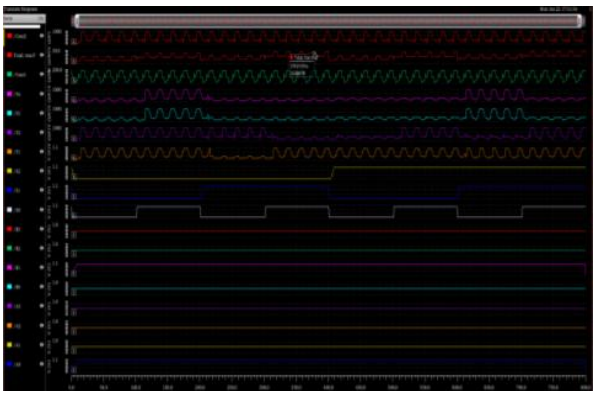


Simulation results of logical block

The below figures show the complete schematic design of the 4-bit ALU and the output of the simulation.



Design of complete 4-bit ALU block



Simulation results of 4-bit ALU block

The below table shows the power comparison between the existing model with the proposed model.

	Power report of existing model (mw)[13]	Power of proposed model
AND Gate	0.693	533.939µw
OR Gate	1.493	713.62µw
XOR Gate	1.493	707.584µw
2:1 MUX	3.628	910.727µw
4:1 MUX	12.933	2.05mw
1 Bit Adder	2.076	3.3991mw
Logical Block	19.708	4.0158mw
Arithmetic Block	10.976	5.9414mw
ALU	54.028	23.93mw

The timing analysis of 4-bit ALU is shown in the below table.

	Delay
AND Gate	38.46E-9
NAND Gate	325.0E-12
OR Gate	38.10E-9
NOR Gate	33.10E-9
NOT Gate	28.25E-9
XOR Gate	40.26E-9
XNOR Gate	33.10E-9
2:1 MUX	17.80E-9
4:1 MUX	159.9E-9
1 Bit Adder	78.70E-9
Subtractor	80.11E-9
Comparator	79.00E-9
Logical Block	99.90E-9
Arithmetic Block	139.9E-9
ALU	403.5E-9

VI. CONCLUSION AND FUTURE SCOPE

The 4-bit ALU was constructed utilising complete adder, 4:l and 2:l multiplexers, and gates such as exclusive-or, and, or, and inverter as sub blocks. The ALU performs eight operations in total, four of which are arithmetic and the remaining four are logical. The four logical operations are AND, OR, XOR, and NOT, and the three arithmetic operations are Adder, Subtractor, and Comparator.

When compared to the present ALU, the power is lowered from 54.028MW to 23.93MW, and the design's acquired delay is found to be 403.5E-9. As a result, the power is lowered.

Further testing of the suggested architecture for low on-chip power density is possible. Though good use of the pulsed power source has been made, we propagation delay can be cut even more by making better use of the pulsed power supply as a VDD source. Checking noise margin and current at different nodes can also improve the performance of the suggested design. As a result, the FinFET-based architecture may be used for a variety of applications, including communication and biomedical processing cores. It is possible to create higher bit ALUs and more complicated processing circuits using this ALU in the future. Finally, an alternative to conventional CMOS circuits has been demonstrated based on lower power, shorter latency, and quicker devices. Other error detection and correction codes, such as Reed Solman and Goley codes, can be implemented with the suggested circuits to provide high performance, low power, and fault secure codes.

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