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Research Paper

Design and Simulation of BSV81 n Channel D MOSFET Single Stage Amplifier for High Frequency Application, Low Output Resistance and Large Bandwidth

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Abstract
The main drawback of Junction Field Effect Transistor (JFET) is that its gate must be reverse bias for proper operation of the device, from which it can only be operated with negative gate operation for n-channel and positive gate operation for p-channel, this means that it can only goes with depletion-mode operation. However, MOSFET can be operated in both enhancement and depletion mode operation In this paper BSV81 n-channel D-MOSFET Single Stage Amplifier was design and the points which determined its output and transfer characteristics, the frequency response and bandwidth of the amplifier were also determined and discussed graphically using Multisim 14.2 simulator. The results obtained characterized the amplifier with high frequency application, low output resistance and large bandwidth.
Keywords: *Amplifier, Simulation, BSV81 D MOSFET n Channel, Single Stage.*

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I. Introduction

A metal oxide semiconductor field effect transistor (MOSFET) is a field effect transistor (FET) with an insulated gate where the voltage determines the conductivity of the device; it is widely used for switching and amplifying electronic signals in the electronic devices, it is a three terminal device such as source, gate, and drain, there are two classes of MOSFETs depletion mode and enhancement mode each class is available as n- or a p-channel, giving a total of four types of MOSFETs (Brotherton, 2013). They have much higher input impedance compare to JFET, they have high drain resistance due to lower resistance of channel, they are easy to manufacture and they support high speed of operation compare to JFETs.

The Bipolar Junction Transistor (BJT) is a current driven device (in contrast, MOSFET is voltage driven) that is widely used as an amplifier, oscillator, or switch, amongst other things, in either case the current's direction in the base is the same as the collector (Chitode, 2020).

Many authors carried out researchers on MOSFET using different simulators software packages, some of them are: Loan *et al*., (2010) carried out research on a Novel Partial-Ground Plane Based MOSFET on Selective Buried Oxide: 2-D Simulation Study, an extensive simulation study, the comparative analysis of the key characteristics of the PGP SELBOX, the SELBOX, and the conventional silicon-on-insulator (SOI) devices has been performed using the 2-D device simulator Medici, the simulations have revealed that the PGP SELBOX and the SELBOX structures are more thermally efficient than the conventional SOI device, Further, the magnitude of the short channel effects (SCEs) is lower in the PGP SELBOX in comparison to the SELBOX device.

Chauhan *et al*.,(2013) carried out research on BSIM compact MOSFET models for SPICE simulation they found that BSIM3 and BSIM4 are threshold voltage based bulk MOSFET models while BSIM6 is charge based bulk MOSFET model, which include physical effects such as mobility degradation, current saturation, high frequency models and also BSIM6 has been developed especially to address symmetry around $V_{ds} = 0$, thus providing smooth higher order derivatives . Zhang *et al*., (2018) carried out research on Simulation Study of a Power MOSFET With Built in Channel Diode for Enhanced Reverse Recovery Performance, the proposed MOSFET is able to deliver superior reverse recovery characteristics, including reductions in reverse recovery charge (QRR) and peak reverse recovery current (IRRM) by a factor of ~4.2 and ~2.6, respectively, the

breakdown voltage (232 V) of the proposed MOSFET is the same as the conventional MOSFET, the on resistance of the proposed MOSFET (8.5 mΩ·cm2) is only slightly increased compared with conventional MOSFET (8.0 mΩ·cm2), the gate to drain charge (QGD) and gate charge (QG) are reduced by a factor of ~7.2 and ~3.9, respectively, significantly improved figures of merit (RON×QG and RON×QGD reduced by a factor of ~3.7 and ~6.8, respectively) are obtained in the proposed MOSFET, the device concept and characteristics are systematically analyzed with numerical TCAD simulations.

Buvannesswari and Balamurugan,(2019) carried out research on 2D analytical modeling and simulation of dual material DG MOSFET for biosensing application, the expression for surface potential is obtained by solving the 2D Poisson's equation using a parabolic potential approach, the threshold voltage is determined from the minimum surface potential model , sensitivity is computed in terms of relative change in the threshold voltage and it is derived using the model, the influence of various device geometrical parameters like length and thickness of the nanocavity on the sensitivity has been investigated. Further, a comparison of the sensitivity of DG MOSFET and DMDG MOSFET has also been made and the derived results are validated against TCAD simulation results.

Shintani *et al* ., (2018) carried out research on Surface-Potential Based Silicon Carbide Power MOSFET Model for Circuit Simulation the proposed model is constructed in a surface potential based framework by considering the physical structure and behavior of vertical power SiC MOSFETs, the proposed model represents both I-V and C V characteristics from weak inversion to the high power region, in addition, the proposed model calculates the channel mobility degradation due to SiC/SiO2 interface traps, which significantly affects the circuit performance through experiments using a commercial SiC power MOSFET, excellent agreements are obtained between measurement and simulation in I-V and C-V characteristics at various temperatures for wide power ranges up to 1 kW, the transient behavior of a double pulse tester is also well reproduced within a timing error of 12.6 ns even under the high temperature.

Roy and Asenov, (2010) carried out a research on Simulation of Statistical Aspects of Charge Trapping and Related Degradation in Bulk MOSFETs in the Presence of Random Discrete Dopants in their research the distribution of fractional current change and threshold voltage shift in an ensemble of realistic 35 nm bulk negative-channel metal oxide semiconductor field effect transistors caused by charge trapping on stress generated defect states at the Si/SiO_2 interface is studied using 3-D statistical, atomistic simulations which in conjunction with strategically positioned traps could result in rare but dramatic changes in the transistor characteristics . However some of the simulators have difficulties for beginners, in that case Multisim can be used for simplicity and acceptable accuracy. The paper came up with a design of BSV81 n channel D MOSFET Single Stage Amplifier, this involves determination of the points at which BSV81 n channel DMOSFET operate output and transfer characteristics with the help of curve, frequency respond and bandwidth of the amplifier using Multisim 14.2 simulator.

II. Design

2.1 Points for BSV81 n Channel D MOSFET Operation

In order to analyze the BSV81 n Channel D MOSFET operation following points were noted as shown figure 1:

(i) The source to drain current is controlled by the electric field of capacitor formed at the gate.

(ii) It is possible to operate D-MOSFET with positive or negative gate voltage.

(iii) Negligible gate current flows whether positive or negative voltage is applied to the gate (Mehta &Mehta, 2008).

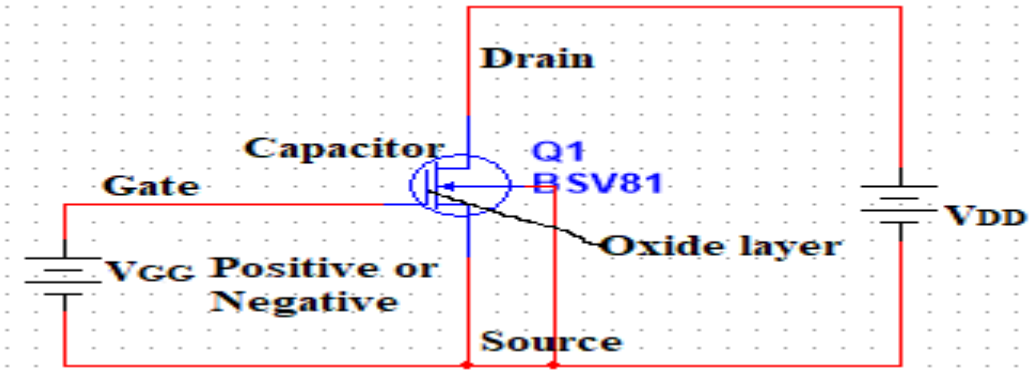

Figure1: n- Channel D- MOSFET

2.2 BSV81 n Channel D MOSFET output and Transfer Characteristic

The output and transfer characteristics for BSV81 n Channel D MOSFET can be explained with the help of curve where as under:

(i) The point on the curve where $V_{GS} = 0, I_D = I_{DSS}$ is expected because I_{DSS} is the value of I_D when gate source terminals was shorted, that is $V_{GS} = 0$ (output characteristic).

(ii) As V_{GS} goes negative I_D decreases below the value of I_{DSS} till it reaches zero when $V_{GS} = V_{GS(off)}$ (transfer characteristic).

(iii) When V_{GS} goes positive I_D increases above the value of I_{DSS} till maximum allowable value of I_D given on the data sheet of BSV81 n Channel D MOSFET (transfer characteristic) (Mehta &Mehta, 2008).

2.3 Zero bias of BSV81 n Channel D MOSFET Amplifier

Any among the following methods can be used for D MOSFET biasing: (i) Gate bias (ii) Self bias (iii) Voltage divider bias (iv) Zero bias. (Mehta &Mehta, 2008). However, zero bias method was chosen for this work as it is widely used in D MOSFET circuits. Note that for the D MOSFET zero bias circuit, the source resistor (R_S) is not necessary since the value of V_S is 0V (Mehta &Mehta, 2008). To form midpoint biasing, the value of R_D is so selected such that $V_{DS} = V_{DD}/2$ and operating point (Q point) can be found using the relation as follows;

$$V_{DD} = I_D R_D + V_{DS}$$

$$\therefore R_D = \frac{V_{DD} - V_{DS}}{I_D} \quad (1)$$

But

$$I_D = I_{DSS}\left\{1 - \frac{V_{GS}}{V_{GS(off)}}\right\}^2 \text{ at shorted gate source voltage } V_{GS} = 0V$$

$$\therefore I_D = I_{DSS} \quad (2)$$

For midpoint bias;

$V_{DS} = \frac{V_{DD}}{2}$, from the graph of figure 5 we have, $I_{DSS} = 0.005939\text{mA}$ and $V_{DD} = 1.5\text{V}$.

$\therefore$ the values of $I_D = I_{DSS} = 0.005939\text{mA}$ and $V_{DS} = \frac{V_{DD}}{2} = \frac{1.5}{2} = 0.75\text{V}$, these two values are the operating point of the circuit and substituting these values into equation one will give;

$R_D = \frac{V_{DD} - V_{DS}}{I_D} = \frac{1.5 - 0.75}{0.005939} = 126.3k\Omega$ and $R_G = 100k\Omega$ usually selected .

This is the d.c. equivalent circuit which will determine the operating point that is d.c. bias levels for the circuit while in an a.c. equivalent circuit which determines the output voltage and hence voltage gain of the circuit. Here the designer intentionally selects capacitors that are large enough to appear as short circuit to the a.c signal (Mehta &Mehta, 2008). In this case an electrolytic capacitor C_{in} (≈100nF) is used to couple the signal to the base of the transistor and a coupling capacitor C_C (≈ 100nF) couples one stage of amplification to the next stage, there is no need a source bypass capacitor C_S which will be used in parallel with R_S to provide a low reactance path to the amplified a.c. signal . The complete amplifier circuit with voltage zero biasing of D MOSFET BSV81 n channel with common source configuration is shown in figure 2.

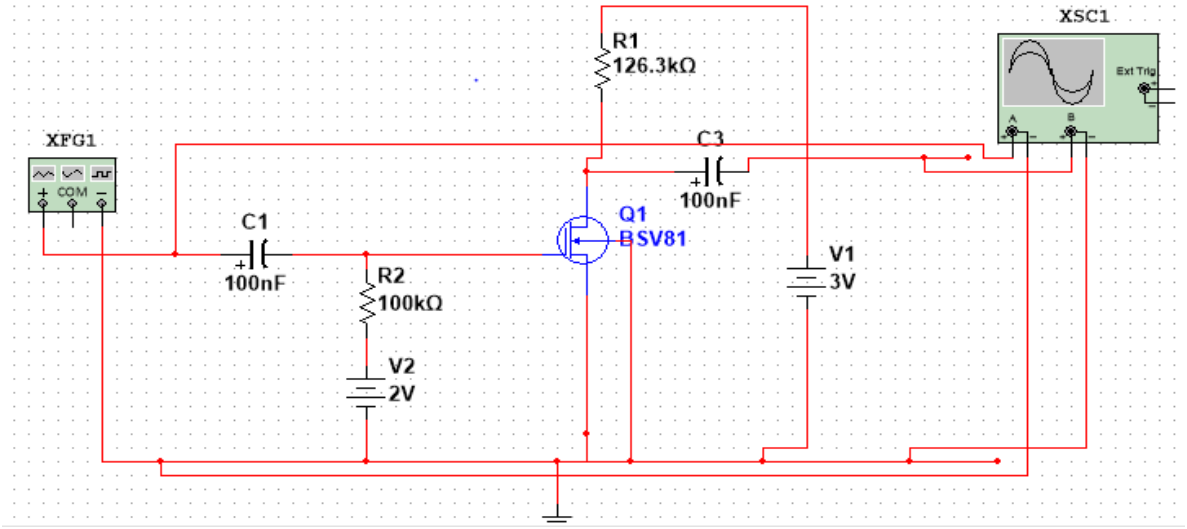

Figure 2: D MOSFET BSV81 n- channel amplifier with common source configuration

III. Simulation

3.1 Determinations of Points for BSV81 n Channel D MOSFET Operation

For BSV81 n Channel D MOSFET operation the following points were determined: **(**i) The source to drain current is controlled by the electric field of capacitor formed at the gate (ii) It is possible to operate BSV81 n Channel D MOSFET with positive or negative gate voltage and **(iii)** Negligible gate current flows whether positive or negative voltage is applied to the gate, the proposed simulation circuit diagrams with negative and positive voltage to the gate is shown in Figure 3 and Figure 4 respectively.

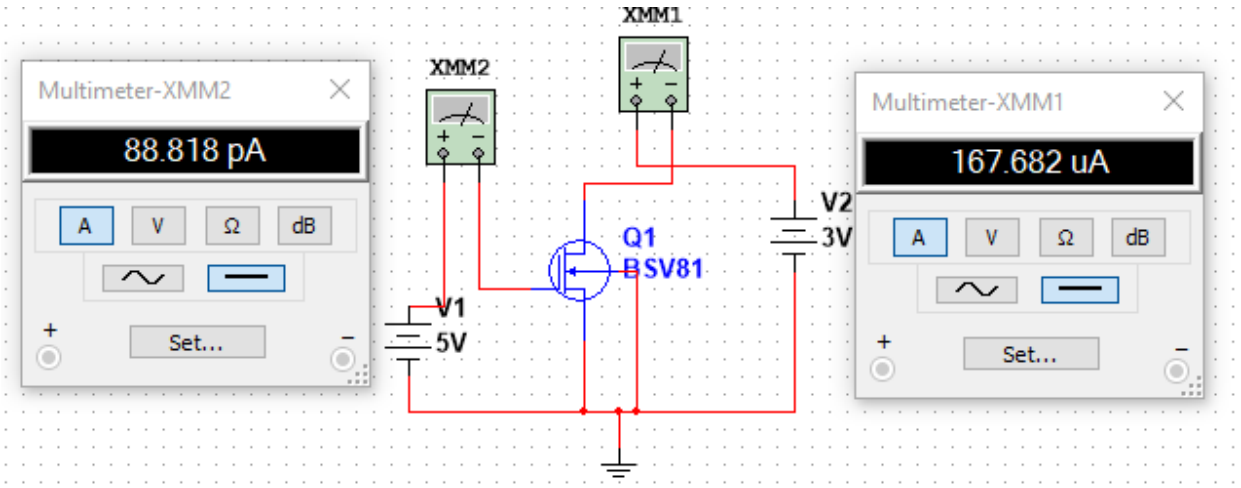

Figure 3: MOSFET with positive voltage to the Gate**,**

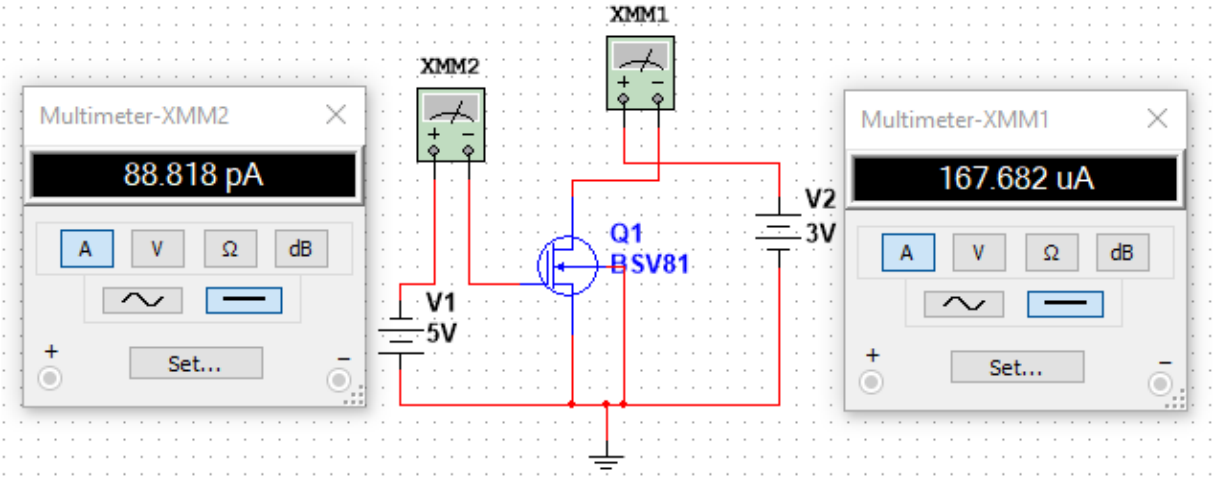

Figure 4: MOSFET with negative voltage to the Gate

3.2 Determinations of BSV81 n Channel D MOSFET Output and Transfer Characteristics

For BSV81 n Channel D MOSFET output and Transfer Characteristic the following were determined with the help of curve as under: **(i)** The point on the curve where $V_{GS} = 0, I_D = I_{DSS}$ is expected because I_{DSS} is the value of I_D when gate source terminals was shorted, that is $V_{GS} = 0$ (output characteristic), **(ii)** As V_{GS} goes negative I_D decreases below the value of I_{DSS} till it reaches zero when $V_{GS} = V_{GS(off)}$ (transfer characteristic) and (iii) when V_{GS} goes positive, I_D increases above the value of I_{DSS} till maximum allowable value of I_D given on the data sheet of BSV81 n Channel D MOSFET (transfer characteristic). The proposed simulation circuit diagrams with shorted gate source voltage and positive gate voltage terminal were shown in Figure 5 and Figure 6 respectively.

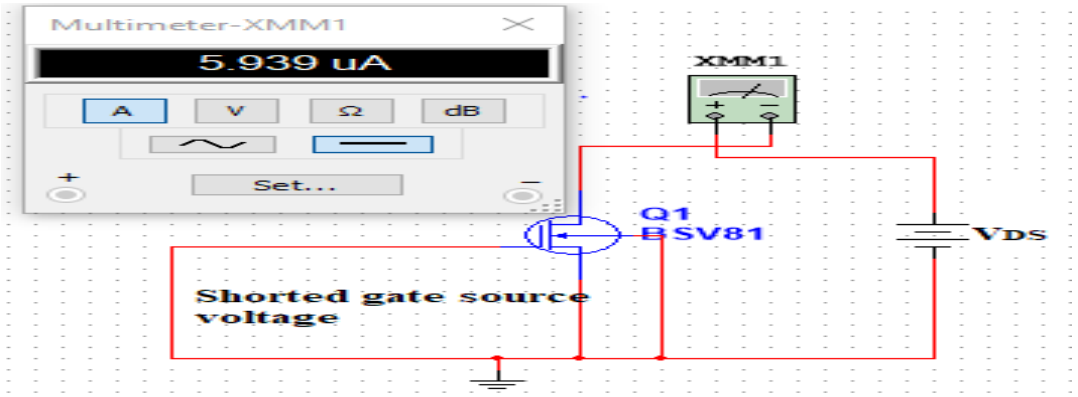

Figure 5: Shorted gate source voltage

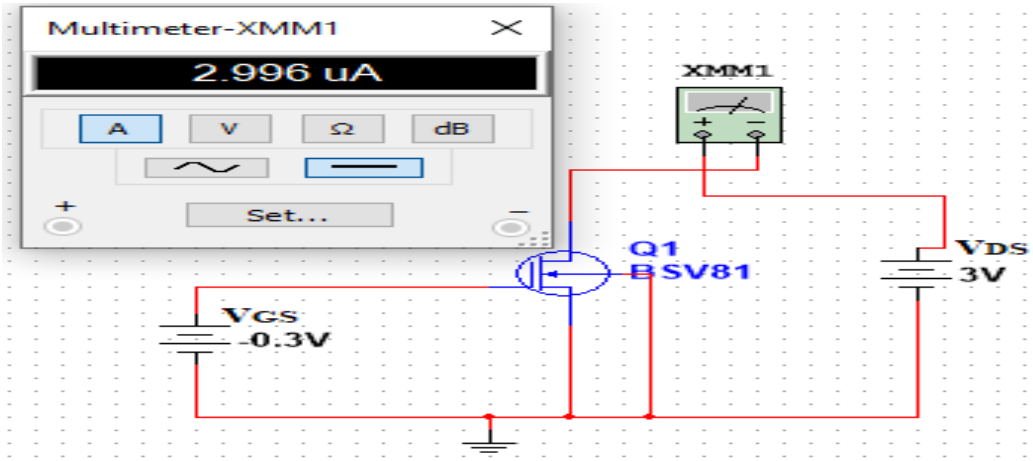

Figure 6: Positive voltage gate terminal

3.3 Determination of frequency response and bandwidth of the amplifier

The frequency response and bandwidth of the amplifier at $V_{DD} = 3V$, $V_{GS} = 1.5V$ and $V_{in} = 2mV$ varying the frequency of the input signal were determined, the proposed simulation circuit diagram is shown in Figure 7.

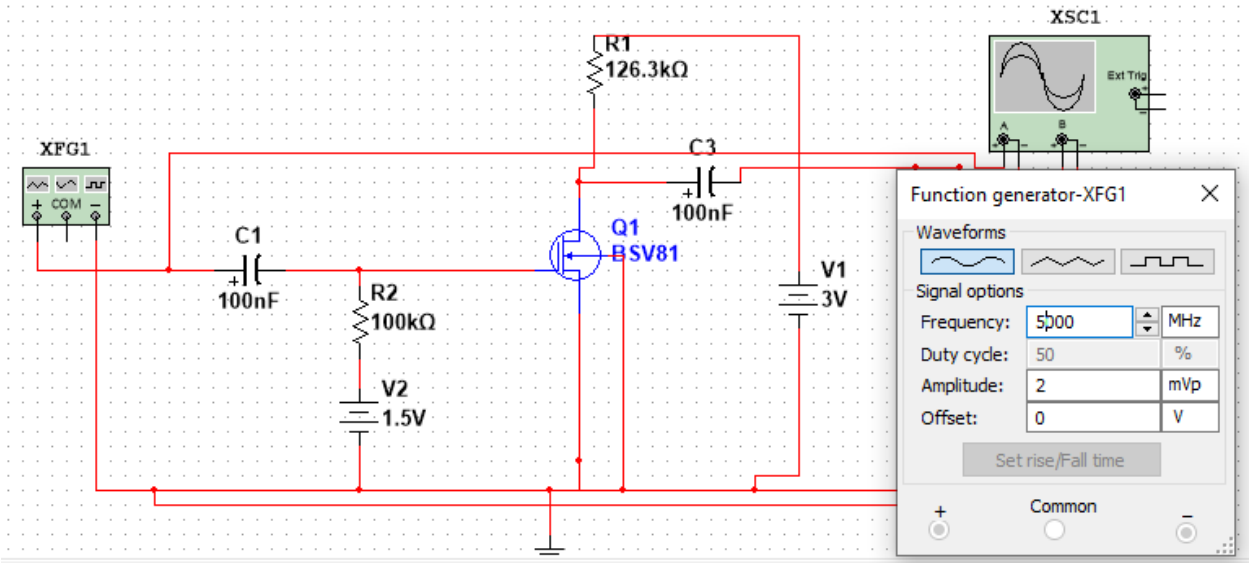

Figure 7: The simulation circuit diagram of a D-MOSFET BSV81 n- channel amplifier witn common source configuration

IV. Results and discussion

4.1 The results For BSV81 n Channel D MOSFET operation points

While keeping the V_{DD}(Volt) fixed at 3V Vary the supply voltage V_{GG}(Volt), 0.0, 0.5, 1.0, 2.0, 3.0, 4.0 and 5.0 from DC power source in steps the corresponding values of drain currents I_D (mA) and gate current I_G(mA) for positive voltage gate terminal was noted down as shown in table 1.

Table 1: The results of drain current I_D(mA) and gate current I_G(mA) for positive voltage terminal

V_{GG}(Volt)	I_D(mA)	I_G(mA)
0.0	0.005939	0.00000000000
0.5	0.013062	0.00000000000
1.0	0.022952	0.00000000000
2.0	0.051034	0.000000022204
3.0	0.088915	0.00000000000
4.0	0.128302	0.00000000000
5.0	0.167682	0.000000088818

Looking at the first data point vertically from the top to down in both column and row of table 1, it shows that increases in positive applied voltage at the positive gate terminal increases the drain currents with a negligible gate current flows, since the gate is positive it induces negative charges in the n channel these negative charges are the free electrons drawn into the channel as suppying voltage on the gate increases the total number of free electrons in the channel and conductivity enhances. Therefore the drain current is controlled by the electric field of capacitor formed at the gate and it is possible to operate BSV81 n Channel D MOSFET with positive voltage gate terminal, this operation is called enhancement mode. For negative voltage terminal at the gate while keeping the V_{DD}(Volt) fixed at 3V Vary the supply voltageV_{GG}(Volt), 0.0, 0.5, 1.0, 2.0, 3.0, 4.0 and 5.0 from DC power source in steps the corresponding values of drain currents I_D(mA) and gate current I_G(mA) for negative voltage terminal at the gate was noted down as shown in table 2.

Table 2: The results of drain current I_D(mA) and gate current I_G(mA) for negative gate voltage terminal

V_{GG}(Volt)	I_D(mA)	I_D(mA)
0.0	0.005939	0.000000000
0.5	0.001587	0.000000011102
1.0	0.000061773	0.000000000
2.0	0.000000088818	0.0000000000
3.0	0.0000000000	0.000000044409
4.0	0.0000000000	0.000000000
5.0	0.0000000000000	0.000000000

looking at the first data point from the top to down in both column and row of table 2, increases in positive supplying voltage at negative gate terminal decreases the drain currents with a negligible gate current flow, is due to the fact that increases in positive supplying voltage at negative voltage terminal lesser number of free electrons made available for current conduction through the n channel because the action with negative gate depends upon emptying the channel of free electrons, the negative gate operation is called depletion mode.

4.2 Results BSV81 n Channel D MOSFET Output and Transfer Characteristic

At shorted gate source voltage vary drain source voltage (V_{DS}) from 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.2, 1.3, 1.4 to 1.5 in steps the corresponding values of drain currents (I_D) was noted down and I - V output characteristics of n channel BSV81 D MOSFET was determined graphically as shown in figure 8.

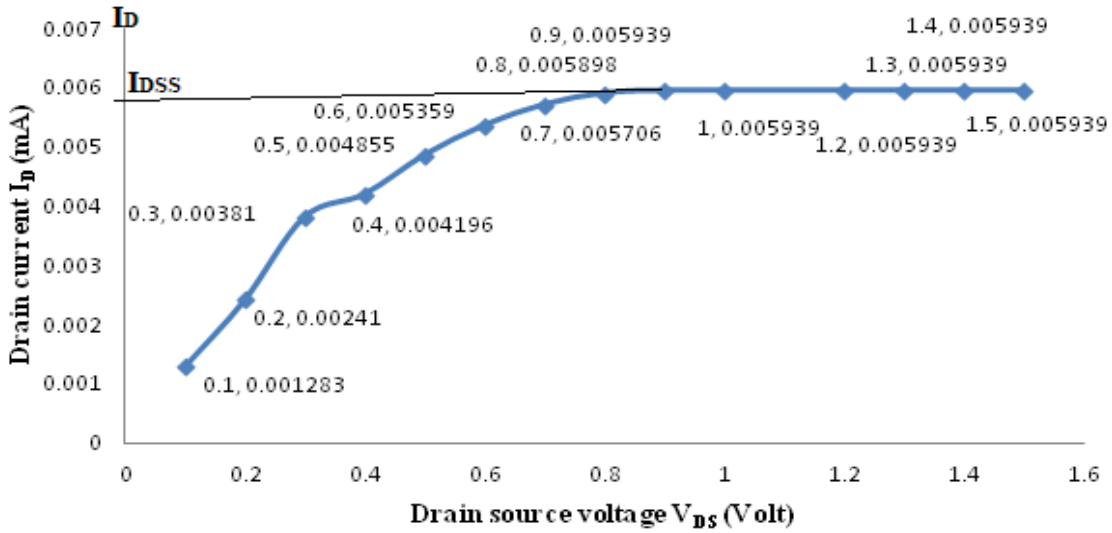

Figure 8 : I-V characteristics of drain source current I_{DS}(mA) against drain source voltage V_{DS}(Volt)

Looking from the graph of figure 5 at shorted gate voltage source the maximum drain current where $I_D = I_{DSS}$ have been measured 0.005939mA at this region values of currents were almost the same, this tell the maximum output current of BSV81 n Channel D MOSFET at shorted gate condition which determined the output characteristic. Also as gate source voltage (V_{GS}) goes negative from -0.1, -0.2, -0.3, -0.4, -0.5, -0.6, -0.7, -0.8, -0.9, -1.0, -1.2, -1.3, --1.4 to -1.5 with positive voltage gate terminal the corresponding values of drain currents I_D(mA) was noted down in steps and I-V characteristics of drain source current I_{DS}(mA) against drain source voltage V_{GS}(Volt) of n channel BSV81 D MOSFET was determined graphically as shown in figure 9.

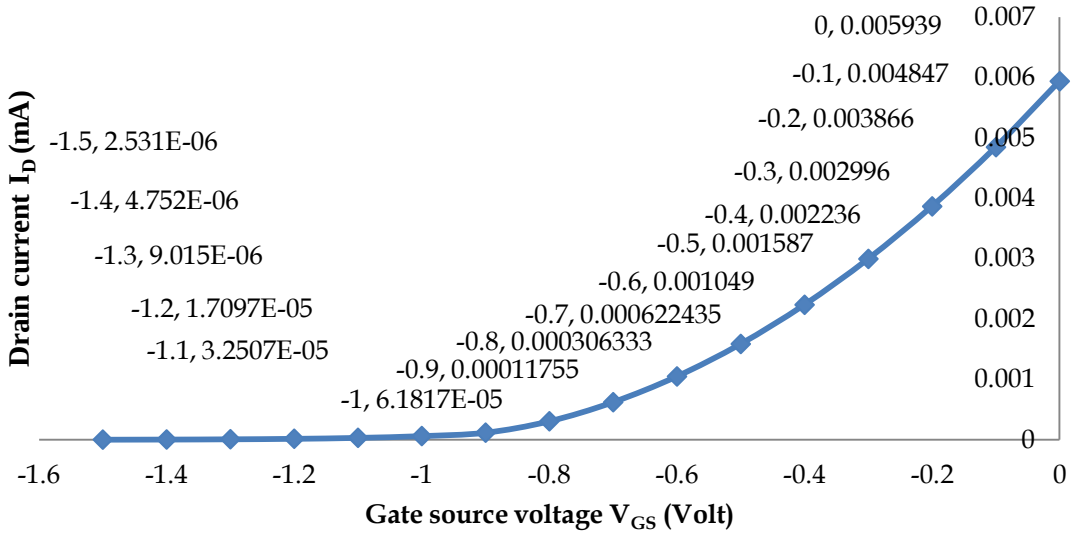

Figure 9: I-V transfer characteristics of drain current I_D(mA) as gate source voltage V_{GS}(Volt) as goes to negative

Looking on the graph of figure 6 from the right to left, it shows that as gate source voltage V_{GS}(mA) goes negative drain current I_D(mA) decreases below the value of maximum drain current at shorted gate source voltage I_{DSS}(mA) till it reaches zero where gate source voltage equal to gate source cut off voltage $(V_{GS} = VGSoff$ at - 1.5V, this change of drain current with respect to the change of VGS as it goes negative called transfer characteristics. When gate source voltage V_{GS}(Volt) goes to positive in steps the corresponding values of drain currents I_D(mA) was noted down at constant drain source voltage V_{DS}(Volt) and I-V characteristics of drain source current I_{DS}(mA) against drain source voltage V_{GS}(Volt) of n channel BSV81 D MOSFET was determined graphically as shown in figure 10.

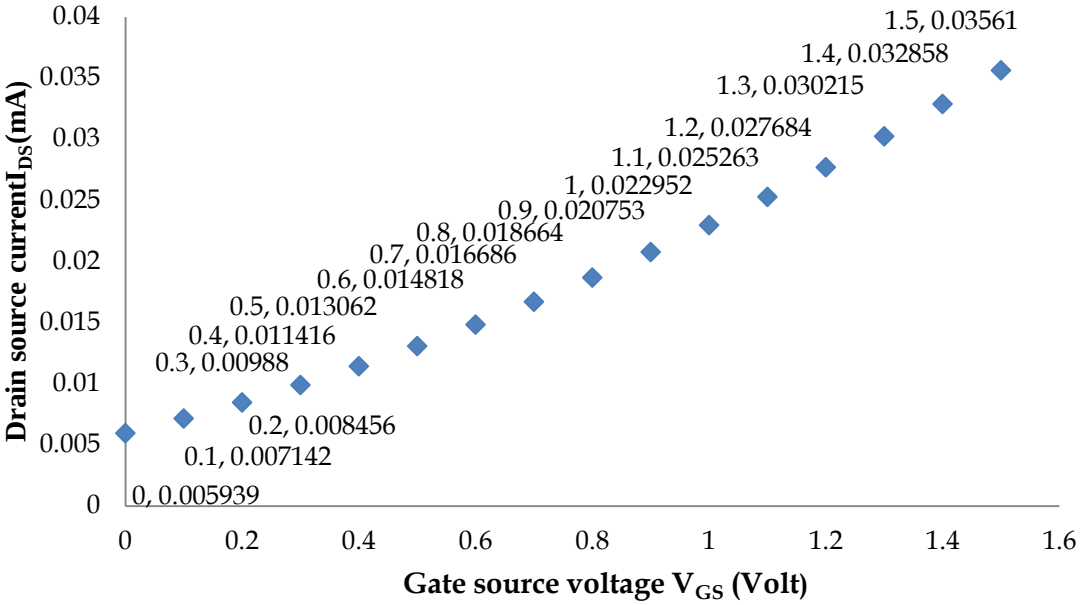

Figure 10: I-V characteristics of drain source voltage (I_{DS}) against gate source voltage (V_{GS}) as it goes to positive

Looking on the graph of figure 7 from the left to right, it shows that as gate source voltage V_{GS}(Volt) goes positive drain source current I_{DS}(mA) increases above it is value at shorted gate source voltage where $I_D = I_{DSS} = 0.005939$mA till maximum allowable value of drain current I_D(mA) given on the data sheet is also called transfer characteristic.

4.3 BSV81 n Channel D MOSFET amplifier frequency response

At constant applied voltages, $V_{DD} = 3V$, $V_{GS} = 1.5V$ and $V_{in} = 2mV$ varying the frequency of the input signal from 10HZ, 14Hz, 100Hz, 200Hz 500Hz, 10KHz, 100KHz, 1MHz, 2MHz, 3MHz, 10MHz, 100MHz, 1GHz, 2GHz, 3GHz, 4GHz, 5GHz, 6GHz, 7GHz, 8GHz, 9GHz, 10GHz, 100GHz, 200GHz, 500GHz, 1000GHz 2000GHz, and 5000GHz, the corresponding amplitude variation in output voltages at different values frequency were determined and the graph of gains against frequencies was plotted as shown in Figure 11.

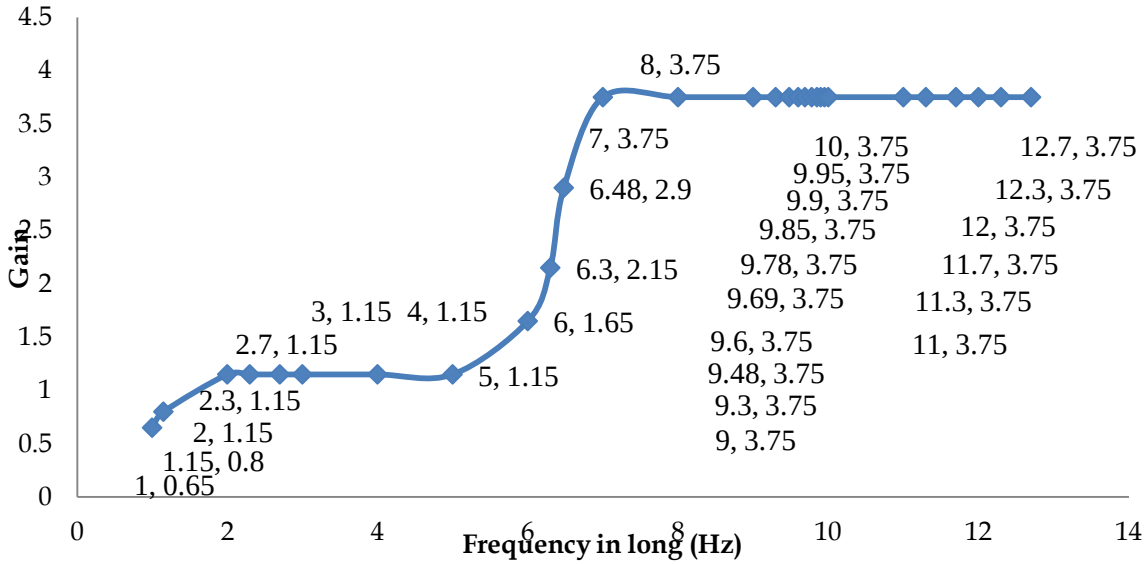

Figure11: The graph of gains against frequencies response of BSV81 n Channel D MOSFET amplifier

Looking at first data point from the left to the right of the horizontal axis of figure 10 graph, the voltage gain of the amplifier increases with increases of the signal frequency, it is clear that at frequency log 1 the gain is 0.65 and from the frequency of log 8 which is lower cut off frequency to the infinity the gain is maximum

3.75 remain constant this characterize the amplifier with high frequency applications low output resistance and large bandwidth.

V. Conclusions

The BSV81 n channel D MOSFET Single Stage Amplifier was design, the points which determined the BSV81 n channel D MOSFET operation were determined, with the help of curve the output characteristics, transfer characteristics, the frequency response and bandwsidth of the amplifier were also determined and discussed graphically using Multisim 14.2 simulator, the results characterized amplifier with high frequency application, low output resistance and large bandwidth.

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