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Research Paper

Design and Analysis of Basic AND Wilson Current Mirror IN 45nm AND 180nm CMOS Technology

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Abstract: *This paper presents a comparative study on the design and analysis of Basic Current Mirror (BCM) and Wilson Current Mirror (WCM) circuits in two different CMOS technology nodes namely 45 nm and 180 nm using cadence virtuoso simulation tool. Current mirrors are fundamental building blocks in analog and mixed-signal integrated circuits and play a critical role in current-mode signal processing and polish applications. The paper begins with an overview of CMOS technology and the basics of current mirrors. Laterthe paperdemonstrate the special design and implementation of Basic Current Mirrors and Wilson Current Mirrors models in both 45 nm and 180 nm technology nodes. The performance of these current mirrors is analysed in terms of key parameters including mirroring accuracy, output impedance, and power consumption.*

Keywords: *Basic current mirror, Wilson Current mirror, virtuoso, mirroring accuracy.*

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I. INTRODUCTION

Current mirror is two terminal circuit, in which the current at output is not dependent on the output terminal voltage but on the reference current i.e., current at input[2]-[11]-[12]. The input current is mirrored at output using pair of transistors. In addition to producing replica of input current, current mirror can also modify the current by attenuating or amplifying it. Current regulated current source is another name for it. The resistance at the output of an ideal current mirror is infinite with zero input impedance to draw or generate constant current over different voltages as it denotes that input current is dependent on input voltage but the output current is not. However, to keep device in saturation, finite output resistance and limited output voltage could also suffice[2]. Various advancement in the technology of CMOS design integrated most of the circuits in the same chip who all are working on very low supply voltage like radio frequency processor and various sensor like temperature and baseband signal processing circuit require very low voltage supply. Getting a very large impedance and wide output range and swing is the important parameter when working on the very low input voltage[7]. A very suitable and simple solution is the application of current mirrors using series and parallel connected CMOS transistors. Depending on the implementation these CMs offer an increased output impedance while the output voltage swing is only slightly decreased or even equal for cascode implementation. This improvement can be reached when forcing transistors to operate in triode region, which makes an application of these current mirrors possible for aggressively scaled submicron CMOS technologies that can operate only at low voltage supplies because of their low breakdown voltages[7].

Basic current mirror topologies which are developed based on MOSFET technology are analyzed and simulated here with comparisons. Different technology nodes 45nm and 180nm are used to elaborate these structures for exploration of the current mirror using the Cadence Virtuoso simulation tool[1].

MOS devices can be applied to design current mirror. While using MOS devices, cascoding techniques are used to increase the output resistance because MOS devices mostly deploy small channel length and with decrease in this channel length the output impedance also decreases.

In basic NMOS current mirror configuration. Depending on the design and requirements, additional components or circuitry might be added to improve accuracy, linearity, and other performance parameters[12]. The Wilson current mirror, as mentioned earlier, is one example of a more advanced current mirror configuration that uses multiple MOSFETs to enhance the accuracy and linearity of the mirrored current. Basic PMOS current mirror depends on design requirements and circuit performance goals, additional components or circuitry may be incorporated to enhance accuracy, linearity, and other performance parameters. Current mirror is used as a source of active load in a variety of applications, such as operational amplifiers, Data converters,

current conveyer etc. Wilson, is an improved mirror circuit configuration designed to provide a more constant current source or sink. It provides a much more accurate input to output current gain[2].

1. LITERATURE SURVEY

In this paper, different current mirror topologies are realized and analyzed using MOSFET and FinFET devices and compared their parameters. The main aim is to seek the performance of FinFET in analog circuits. FinFET current mirrors are realized with the basic topologies i.e., Simple current mirror, Wilson current mirror, Improved Wilson current mirror, and Cascode current mirror along with 180 nm, 90 nm, 45 nm, and 18 nm technology nodes using the Cadence Virtuoso Simulation tool [1].

In this paper, various current mirror topologies are surveyed based on technology of 90nm. The performance parameters of these technologies like output current, impedance, transconductance and transfer characteristics are also discussed. High performance of analog structures depends on parameters like output resistance and settling time of current mirrors. High operation speed, small area and less power dissipation are characteristics of circuits built using current mode [2].

In this work, 4 topologies of the current mirror have been explored with the primary motivation of reduction in power consumption towards nw. Simulation result of operational transconductance amplifier (OTA) with mod-Wilson current mirror combination attains the minimum power of 437nW and achieves the input-referred noise to 2.55μV/√Hz which is minimum among different topology of the current mirror. The different circuit topologies of internal components are capable to provideacceptable value. The circuit has been optimized with supply voltage ±0.5V for a midband gain [3].

This paper presents the design of Operational transconductance Amplifier using Wilson current mirror with enhanced performance in comparison to the OTA using simple current mirror. Wilson current mirror is the modified form of the Simple current mirror. It has improved and better characteristics as compared to the earlier one and hence enhances the performance of the circuit in which it is used. Circuit is designed and simulated using Cadence Virtuoso at 180nm technology nodes [4].

In this article, a differential amplifier with a moderate gain of 40.56 dB is achieved. The UGF of 46.985 dB and phase margin of 84.15 degrees with a low power consumption of 61.084 uW. It is designed by using 90 nm CMOS technology in CADENCE VIRTUOSO platform by applying a supply voltage of 1.2 V with an ICMR of −296.098 mV–1.158 V. The post-layout simulations are also carried out and the results are being compared to the pre-layout results. Finally, a comparison is also drawn with some recent works [5].

This paper presents a simple and easy-to-use method allowing to improve output swing of regulated cascode CMOS current mirror with short channel devices. It is based on matched offset voltage generators, implemented simultaneously at the input and output of the current mirror. This paper presentsa concept of circuit implementation, a mathematical description of the optimal value of voltage offset, and simulation results in 40nm process [6].

This paper highlights the theoretical framework for the operation of current mirror devices and delves into the properties of the folded cascode current mirror. It expounds the simulated results obtained through Cadence, performs a comparison between the results of the two software and concludes by discussing the circuit's prospects [7].

II. PROBLEM STATEMENT

In modern integrated circuit design, current mirrors play a critical role in maintaining precise current matching and biasing in various analog and mixed-signal circuits. In the context of 45nm and 180nm CMOS (Complementary-Metal-Oxide-Semiconductor) technology nodes, two commonly used current mirror configurations are the basic current mirror and the Wilson current mirror[11]. These mirrors serve as essential building blocks for applications like voltage references, operational amplifiers, and analog-to-digital converters. Design and analysis of current mirror with Wilson current mirror in 45nm and 180nm CMOS technology and the parameters such as DC Analysis, AC Analysis, mirroring accuracy, output impedance, power consumption are compared. This project aims to create an efficient and precise current mirror, a crucial building block in analog and mixed-signal circuits.

Mirroring accuracy refers to how close the output current matches the input current that it is supposed to mirror.

Mirroring accuracy(%) = $\frac{I_{out}}{I_{in}} \times 100\%$

Output impedance is a measure of how the output current changes with variations in the voltage at the output.

Output Impedance = $\frac{1}{\mu_n C_{ox} \frac{W}{L} I_{out}}$

Power consumption is the amount of power consumed by the circuit while mirroring a current from one branch to another.

Power consumption= $I_{total} \times V_{supply}$

III. METHODOLOGY

3.1 BASIC CURRENT MIRROR

Designing a Basic current mirror circuit that accurately replicates a reference current using NMOS (N-channel Metal-Oxide-Semiconductor) transistors. The first step is to define the specifications, including the desired reference current and the technology parameters relevant to the design. Next, proper sizing of the NMOS transistors is essential. The mirror transistor should be sized to operate in the saturation region, ensuring consistent drain current even with varying drain-source voltages. Biasing the reference transistor is the subsequent step, which establishes a known current source; this can involve using biasing resistors or other circuits.The working of the current mirror depends on the applied voltage and their process parameters such as aspect ratio. Hence, in Fig. 1 both transistors are identical and their length should be equal (L1=L2) for mirroring. Here, the gate-source voltage of M1 and M2 is equal hence the channel current will be equal. For the proper mirroring operation of the circuit, transistors should remain in the saturation region. Current mirror structures can be made by adding two transistors by their gate and the input side transistor should be diode-connected and the output side transistors will get the required gate-source voltage by this diode-connected transistor. For the current mirror to be working as an amplifier the aspect ratio of M2 should be greater than M1[13]-[16].

M1 corresponds to VGS1 and M2 corresponds to VGS2.Transistors are identical i.e.VGS1 = VGS2, therefore identicaldrain current flows in both, after ensuring that M2 operates insaturation.

Here, the Id1 is given by:

$$I_{d1} = \frac{\beta_1}{2}(V_{GS1} - V_{th})^2 \qquad (1)$$

Now, considering M2 is in saturation, we get at M2 asfollows:

$$I_{d2} = \frac{\beta_2}{2}(V_{GS2} - V_{th})^2 \qquad (2)$$

Here, $I_{D2} = I_O$

The ratio of drain current can be obtained as follows:

$$\frac{I_{d2}}{I_{d1}} = \frac{\beta_2}{\beta_1} = \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} \qquad (3)$$

Therefore, by adjusting the values of W/L, current mirror'soutput current can be changed[6].In order for M2 to remainin saturation, the minimum voltage at output that is requiredin current mirror is VMIN = VGS – Vth. The current mirror'soutput impedance is much like the transistor M2's outputimpedance[7]. Fig.3depicts a schematic diagram of a basic current mirror circuit implemented in a 45nm CMOS technology node. This circuit serves as a fundamental building block for replicating a reference current source and is crucial in variousanalog and mixed-signal applications.Fig.4illustrates the DC analysis of a basic current mirror circuit implemented in a 45nm CMOS technology, allowing for the examination of current replication and biasing characteristics under steady-state conditions. Fig.5 presents the AC analysis of a basic current mirror circuit implemented in a 45nm CMOS technology, enabling the evaluation of its dynamic response and performance characteristics under varying input signals and frequencies. Fig.6 illustrates the output impedance characteristics of a basic current mirror circuit implemented in a 45nm CMOS technology, providing insights into its ability to maintain stable current replication and voltage regulation against load variations.Fig.7 displays the schematic diagram of a basic current mirror circuit implemented in a 180nm CMOS technology, which serves as a foundational component for replicating a reference current source in various analog and mixed-signal applications within this technology node. Fig.8 illustrates the DC analysis of a basic current mirror circuit implemented in a 180nm CMOS technology, providing insights into current replication and biasing characteristicsunder steady-state conditions in this specific technology node. Fig.9 represents the AC analysis of a basic current mirror circuit implemented in a 180nm CMOS technology, enabling the examination of its dynamic response and performance characteristics under varying input signals and frequencies within this specific technology node. Fig.10 showcases the output impedance characteristics of a basic current mirror circuit implemented in a 180nm CMOS technology, providing insights into its capacity to maintain stable current replication and voltage regulation against load variations within this particular technology node.

3.2 WILSON CURRENT MIRROR

Designing a Wilson current mirror, an enhanced version of the basic current mirror circuit that accurately duplicates a reference current using multiple transistors, typically NMOS, to mitigate limitations present in the simple configuration. The first step is transistor sizing; the mirror transistors are optimally scaled to ensure they operate in the saturation region and contribute to improved linearity.To modify the performance of simple current mirror Wilson CM is demonstrated (Fig. 2). It consists of three transistors which one of them is a diode connected to maintain the gate-source voltage for mirroring. Transistor M3 is implemented in such a way that it produces a shunt-series type of negative feedback. Due to this feedback higher output resistance can

be seen in Wilson CM. But this topology comes up with a deficiency of large compliance voltage which should be as low as possible.

Drawback of Wilson CM is that it has not equalled the drain-source voltage of transistors M1 and M2. This is the result of channel length modulation and it causes lesser mirroring accuracy.

The voltages are given as:

$V_{outmin} = V_{th} + 2V_{DSsat}$ (1)

$V_{inmin} = 2V_{th} + 2V_{DSsat}$ (2)

Where $V_{out\,min}$ and $V_{in\,min}$ are the minimum output andinput voltage. V_{th} represents the threshold voltage of thetransistor and its minimum drain-source voltage formaintaining it in the saturation region is given as $V_{DS\,sat}$. Fig.11 illustrates the schematic diagram of a Wilson current mirror circuit implemented in a 45nm CMOS technology, which is an enhanced version of a current mirror designed to improve linearity and output impedance for precise current replication in analog and mixed-signal circuits within this technology node.Fig.12 presents the DC analysis results of a Wilson current mirror circuit implemented in a 45nm CMOS technology, offering insights into its performance with respect to current replication and biasing under steady-state conditions within this specific technology node. Fig.13 represents the AC analysis of a Wilson current mirror circuit implemented in a 45nm CMOS technology, facilitating the examination of its dynamic response and performance characteristics under varying input signals and frequencies within this specific technology node, emphasizing its enhanced linearity and output impedance. Fig.14 illustrates the output impedance characteristics of a Wilson current mirror circuit implemented in a 45nm CMOS technology, highlighting its improved ability to maintain stable current replication and voltage regulation against load variations within this specific technology node. Fig.15 provides the schematic diagram of a Wilson current mirror circuit implemented in a 180nm CMOS technology, showcasing an enhanced CM configuration designed to improve linearity and output impedance for precise current replication in analog and mixed-signal circuits within this technology node. Fig.16 shows the DC analysis results of a Wilson current mirror circuit implemented in a 180nm CMOS technology, offering insights into its performance characteristics related to current replication and biasing under steady-state conditions within this specific technology node. Fig.17 illustrates the AC analysis of a WCM circuit implemented in a 180nm CMOS technology, enabling the examination of its dynamic response and performancecharacteristics under varying input signals and frequencies within this specific technology node, emphasizing itsenhanced linearity and output impedance. Fig.18 depicts the output impedance characteristics of a WCM circuitimplemented in a 180nm CMOStechnology, highlighting its improved ability to maintain stable current replication and voltage regulation against load variations within this specific technology node.

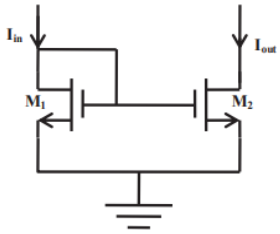

Fig.1 Basic current mirror

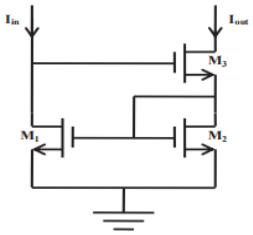

Fig.2 Wilson current mirror

IV. RESULT AND DISCUSSION

Basic current mirror and Wilson current mirror are simulated on 45nm and 180nm technology node using the Cadence Virtuoso tool. The input current has taken for DC analysis as 30μA. Similarly, for DC analysis output voltage is taken to have values of 1.2V for 45nm and 2.5V for 180nm technology. Calculation of output resistance carried out atAC analysis within 1-1MHz range as a log scale of 20 decades.

Analysed DC Response which helps to determine the operating condition of current mirror circuit and helps us to understand whether the mirrored output current closely matches the input current. Analyzed AC Response which helps to determine how the current mirror circuit responds to varying frequencies of input signals. The project aims to compare the performance of these current mirrors with respect to key parameters such as mirroring accuracy, output impedance, power consumption.

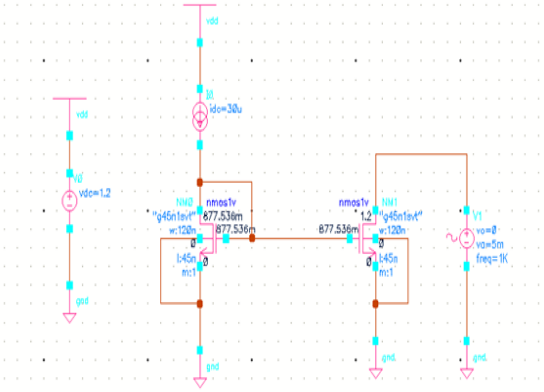

Fig.3 Basic current mirror schematic in 45nm technology

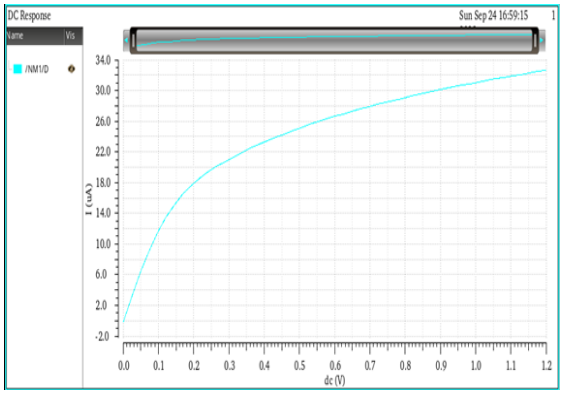

Fig.4 DC Analysis of Basic current mirror in 45nm technology

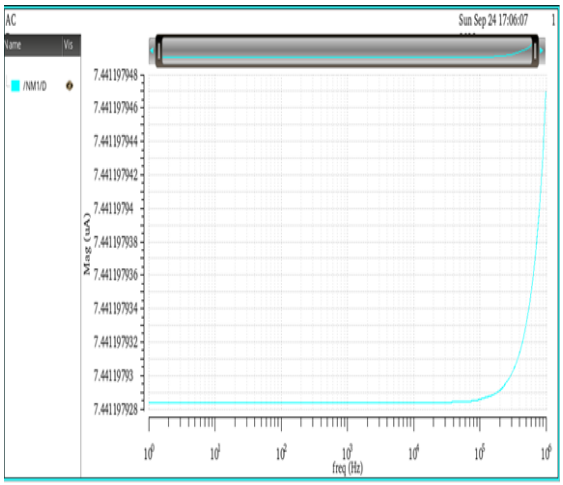

Fig.5 AC Analysis of Basic current mirror in 45nm technology

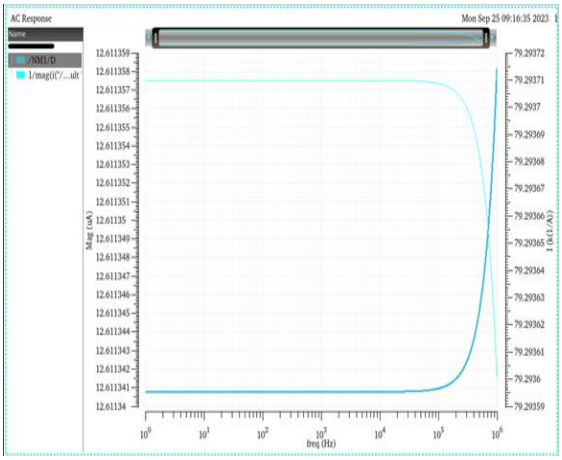

Fig.6 Output impedance of Basic current mirror in 45nm technology

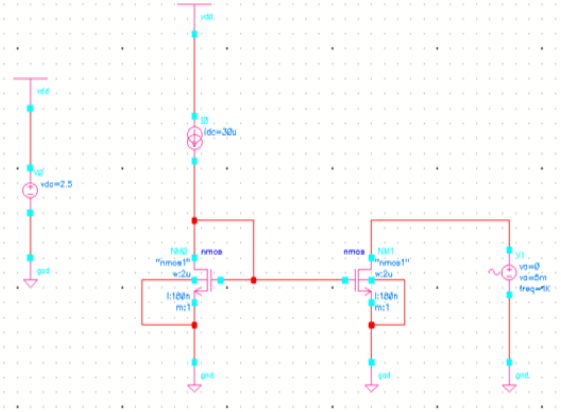

Fig.7 Basic current mirror schematic in 180nm technology

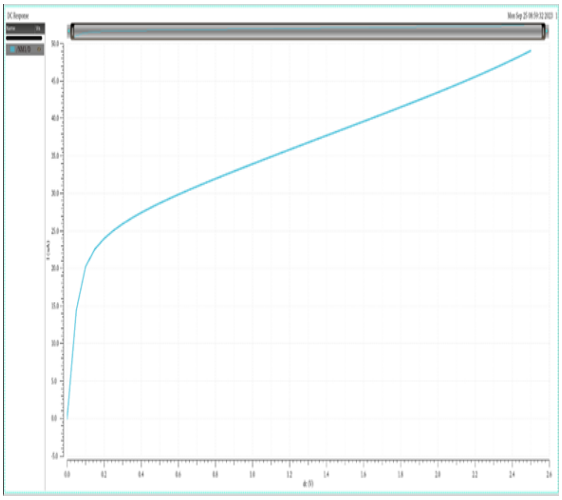

Fig.8 DC Analysis of Basic current mirror in 180nm technology

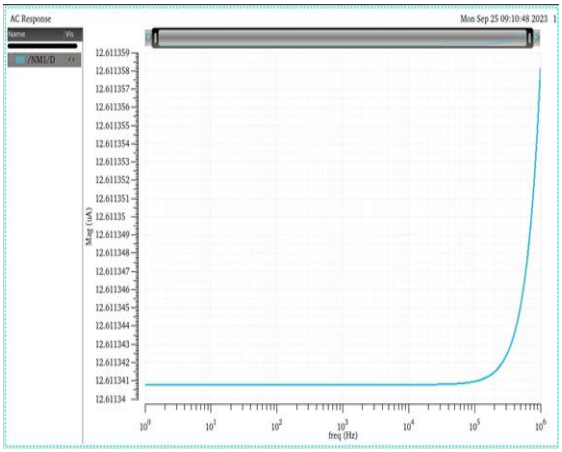

Fig.9 AC Analysis of Basic current mirror in 180nm technology

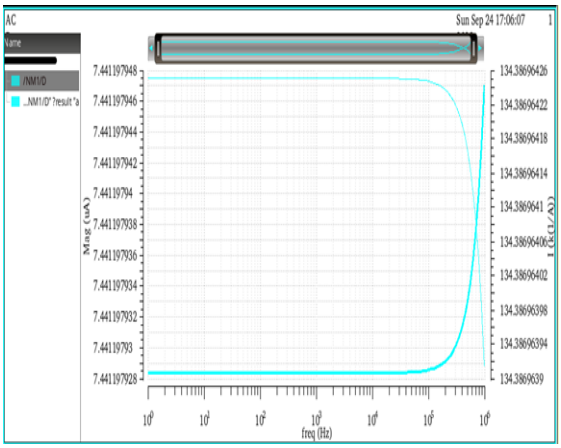

Fig.10 Output impedance of Basic current mirror in 180nm technology

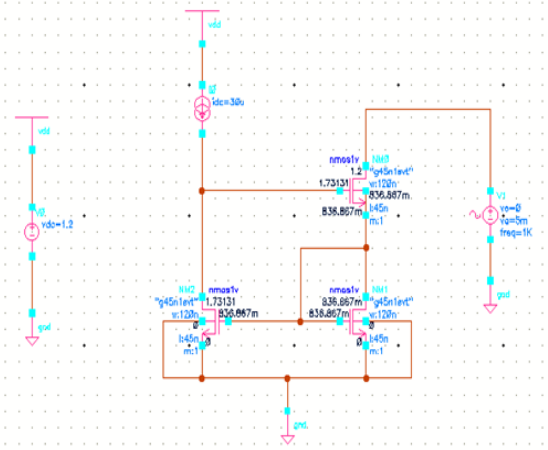

Fig. 11 Wilson current mirror schematic in 45nm technology

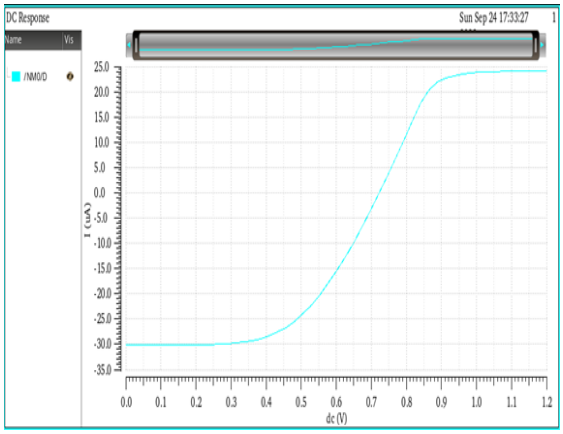

Fig.12 DC Analysis of Wilson current mirror in 45nm technology

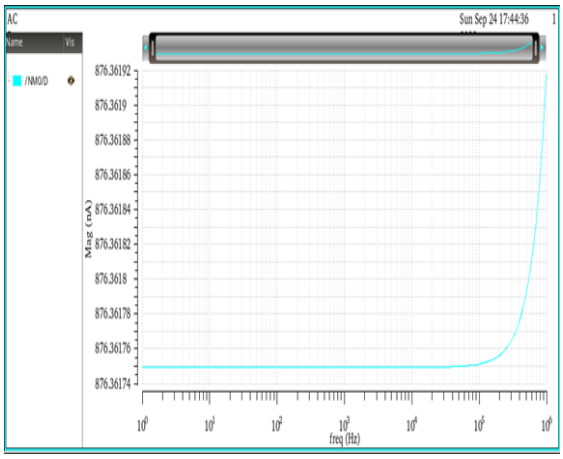

Fig.13 AC Analysis of Wilson current mirror in 45nm technology

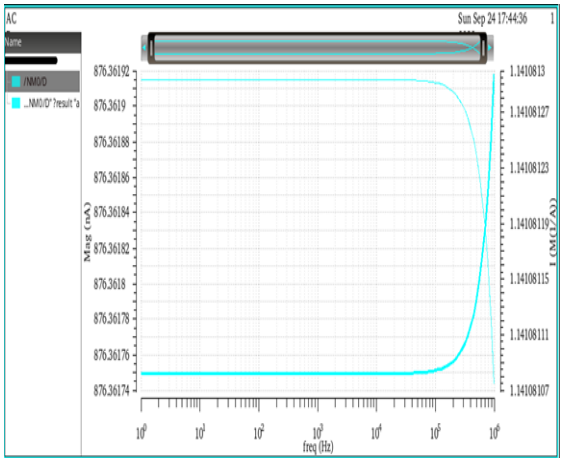

Fig.14 Output impedance of Wilson current mirror in 45nm technology

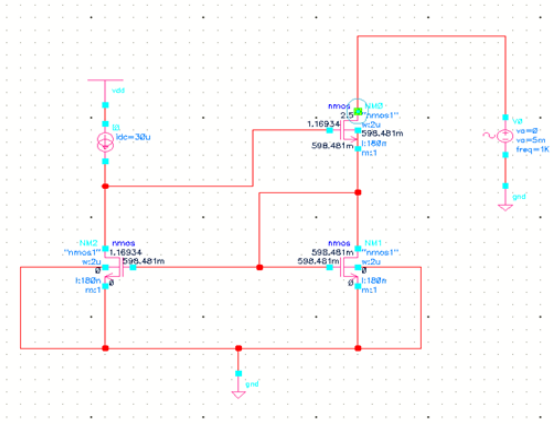

Fig.15 Wilson current mirror schematic in 180nm technology

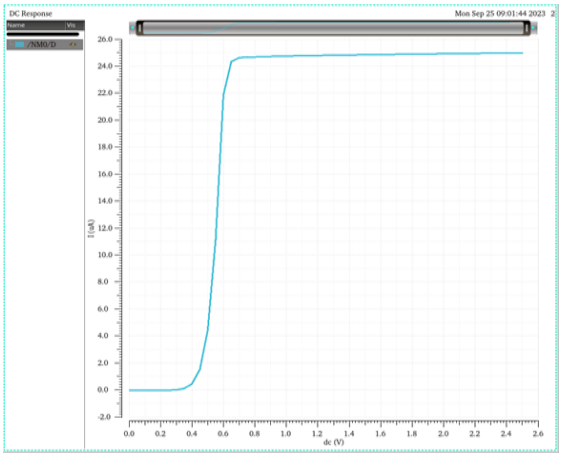

Fig.16 DC Analysis of Wilson current mirror in 180nm technology

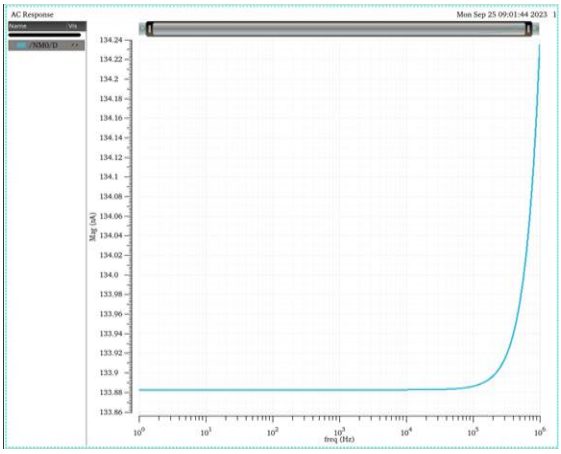

Fig.17 AC Analysis of Wilson current mirror in 180nm technology

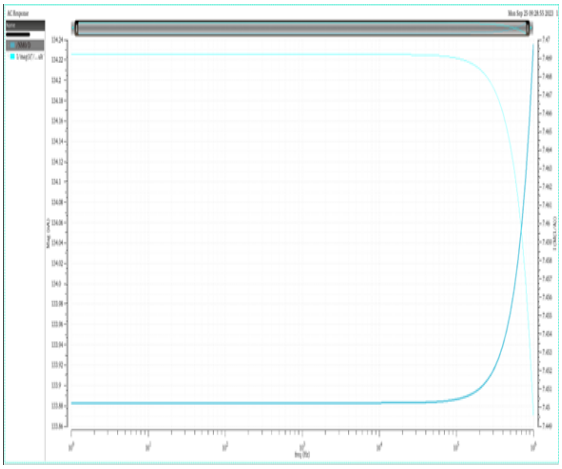

Fig.18 Output impedance of Wilson current mirror in 180nm technology

Topology	Parameter	180nm	45nm
BASIC CURRENT MIRROR	MIRRORING ACCURACY(%)	1.634	1.09
	OUTPUT IMPEDANCE(Ω)	109.28	41.89
	POWER CONSUMPTION(W)	75	36
WILSON CURRENT MIRROR	MIRRORING ACCURACY(%)	0.83	0.81
	OUTPUT IMPEDANCE(Ω)	6.7	1.6
	POWER CONSUMPTION(W)	75	36

TABLE 1. Comparative results for different current mirrors in different technology node

V. CONCLUSION

This paper reports a comparison of various current mirrors at different technology nodes analysed in cadence virtuoso. The comparison between the two technology nodes underscored their distinct advantages and considerations. The 45nm technology demonstrated superior attributes in terms of reduced power consumption and smaller area utilization, making it well-suited for power-sensitive applications. Conversely, the 180nm technology exhibited enhanced linearity and bandwidth, catering to scenarios that demand higher output swing and faster response times.

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